



# A Proposal for the SNS Timing System

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# Timing System Requirements

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- SNS Timing Workshop LANL January 26th 1998
- SNS Timing Workshop BNL May 3-5 1999
- SNS Timing and Synchronization System by R.E. Shafer May 31, 1999
- SNS Beam Diagnostics Workshop LBNL October 13-15 1999

# Timing System Requirements

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- Provides:
  - synchronization among various systems
    - Neutron chopper
    - Linac chopper
    - Linac and Ring RF
    - Injection and Extraction
    - Beam Instrumentation
  - Mode scheduling

# Timing System Requirements

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- Stability:
  - $\sim \pm 5\text{ns}$  (relative to beam in the ring)
- Frequency compliance:
  - ring revolution variations of  $\pm 2\text{ns}$  or  $\pm 2400\text{ ns}$  for the accumulation period should not require changing downloaded delays
- Clock:
  - Must be CW, independent of whether beam is in the ring

# Timing System Requirements

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- Real time event encoding:
  - Ability to encode and transmit 100s of timing signals in real time
- Granularity:
  - 50 ns
- Transmission method:
  - Broadcast transmission on cable or optical fiber of a single encoded clock and trigger signals

# Timing System Requirements

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- Informational events:
  - Ability to distribute informational as well as timing events
- Priority system:
  - Critical timing events are given priority to prevent contention over informational or non critical events
- Bit Error rate:
  - $1 \times 10^{-13}$  = ~1 error/year @ 100 events per cycle

# Beam Macropulse Gate



- Injector beam gate timing is determined by injecting about 1160 turns into the ring
- Ring should be full about 10  $\mu\text{s}$  before extraction
- Beam storage beyond 10  $\mu\text{s}$  leads to more time for instability growth

# Ring Revolution Period



- Ring revolution period is about 841.2 ns
- Revolution period may be adjusted by as much as  $\pm 1$  ns during commissioning and normal operation
- For 1160 turns, fill time can vary by as much as  $\pm 1000$  ns
- To meet this requirement with a fixed frequency clock would require changing the downloaded delays during the cycle
- hence the need for a beam Synchronous clock

# SNS Timing System

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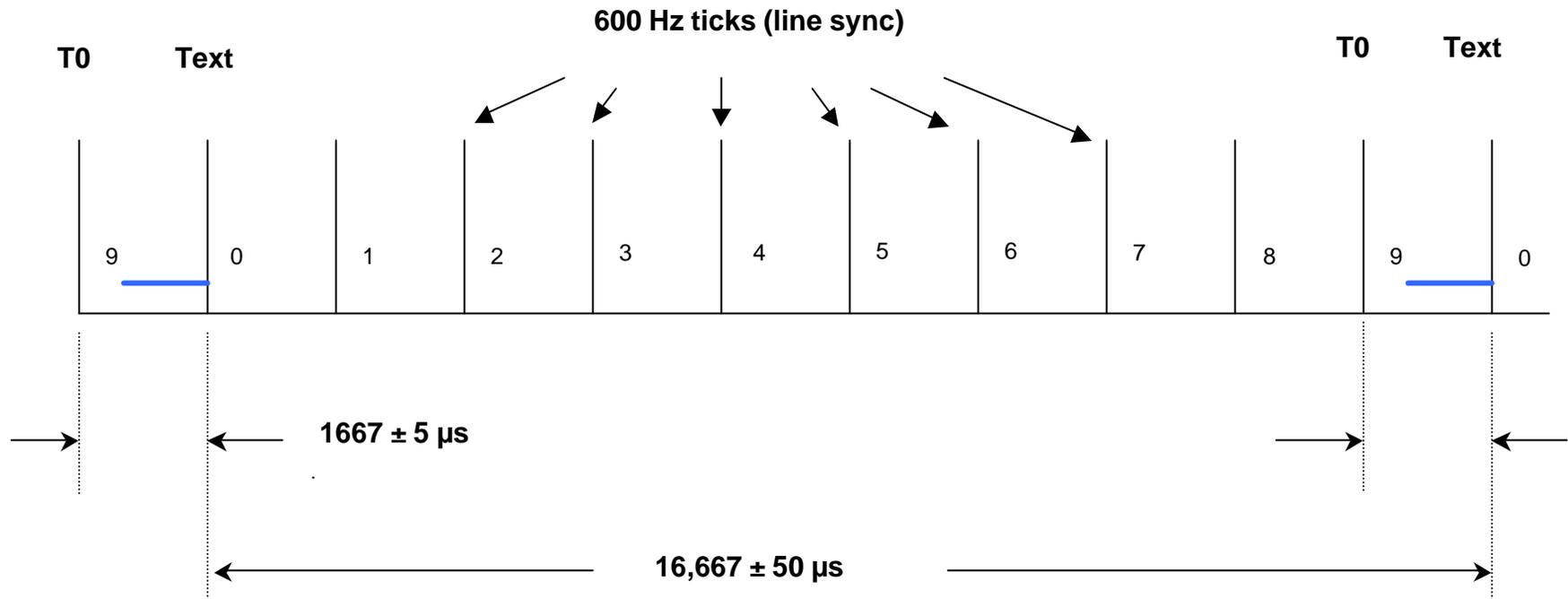
- RHIC Timing system would be the model for SNS Timing system
  - Broadcast Event System
    - One transmitter
    - Many receivers
    - Receivers respond only to events programmed
  - Beam Synchronous
  - Proven technology
  - VME based system

# SNS Timing System

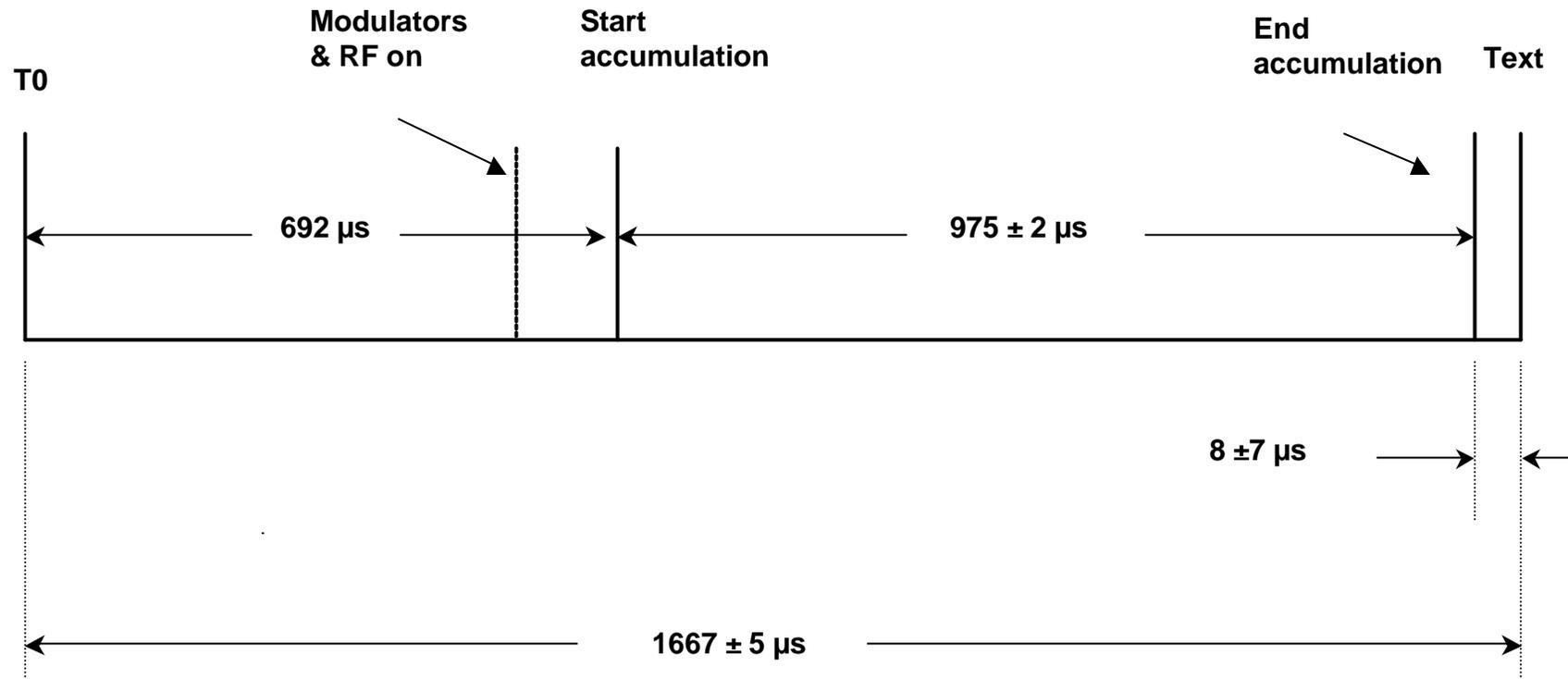


- $F_{\text{rev}}$  of Ring = 1.19 MHz  $\pm$  0.25%
- Beam Sync Carrier Frequency =  $16 * f_{\text{rev}} = 19.02$  MHz
- 64 direct pulse inputs (expandable)
- maximum of 255 events can be defined
- Jitter < 2 ns Pk to Pk
- granularity 52 ns
- 630 ns with contention

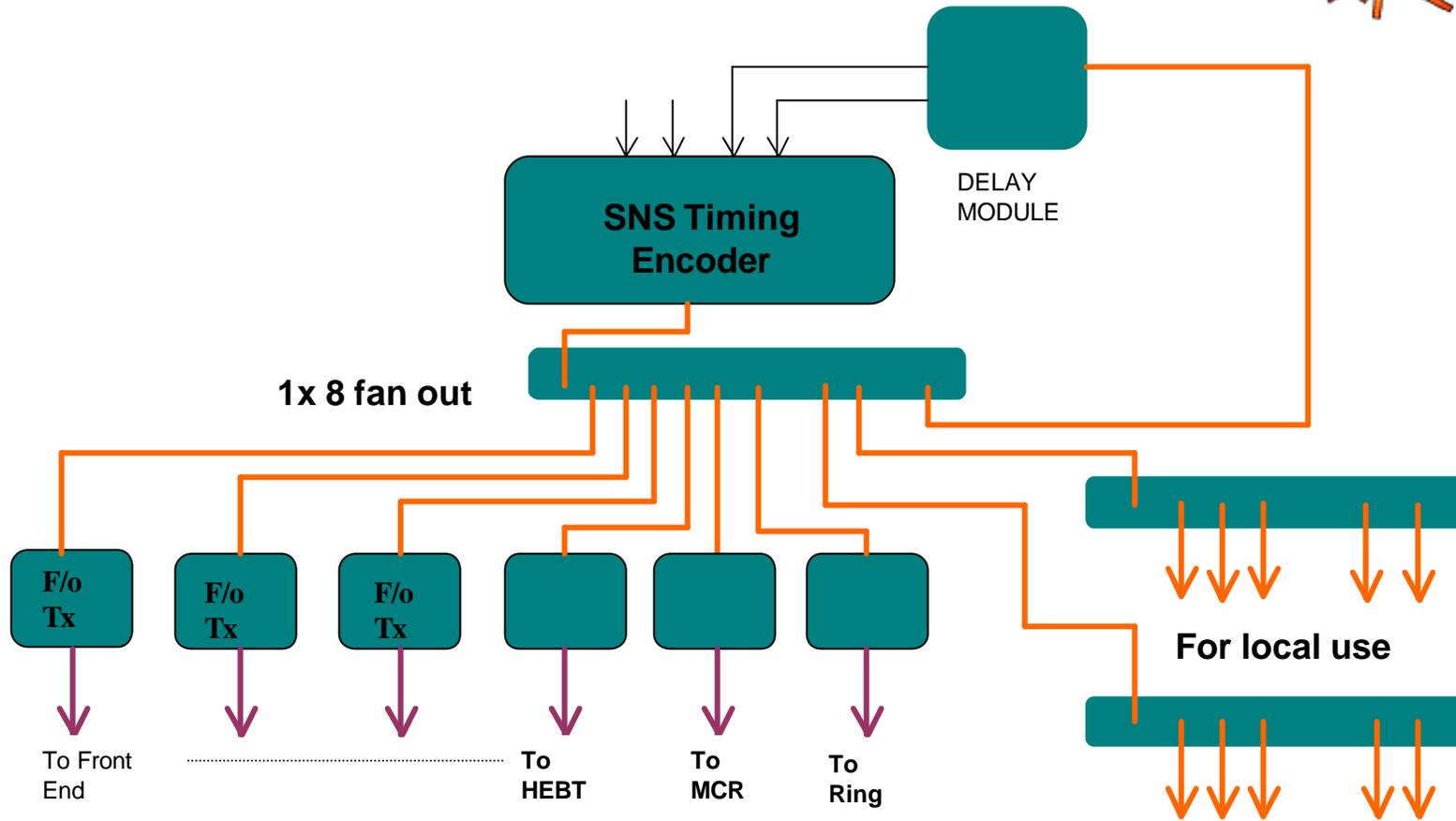
# Typical 60 Hz line cycle



# Detail of accumulation cycle



# SNS Timing Distribution



Multimode fiber

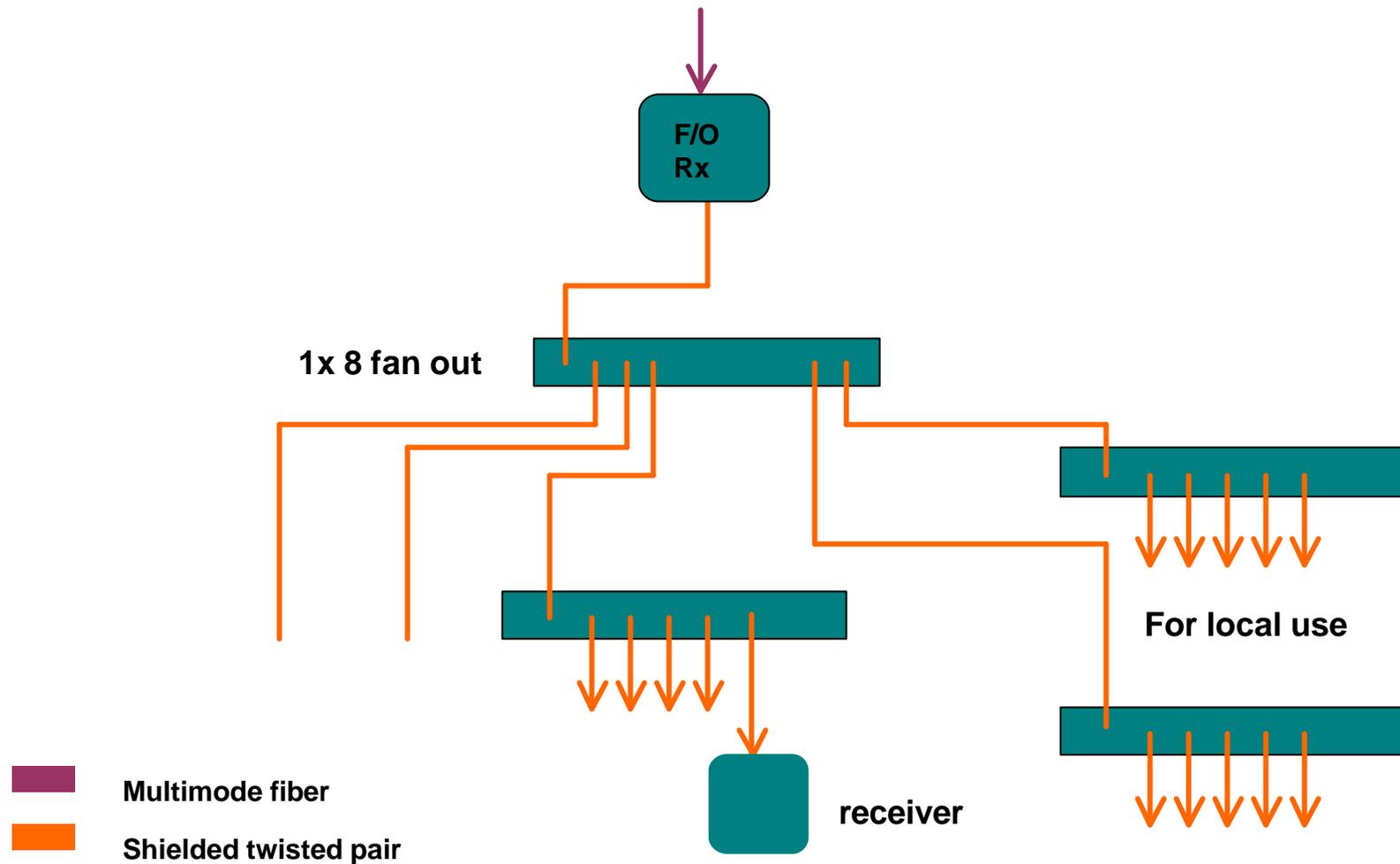


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SNS Timing Proposal

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# Typical Local Distribution



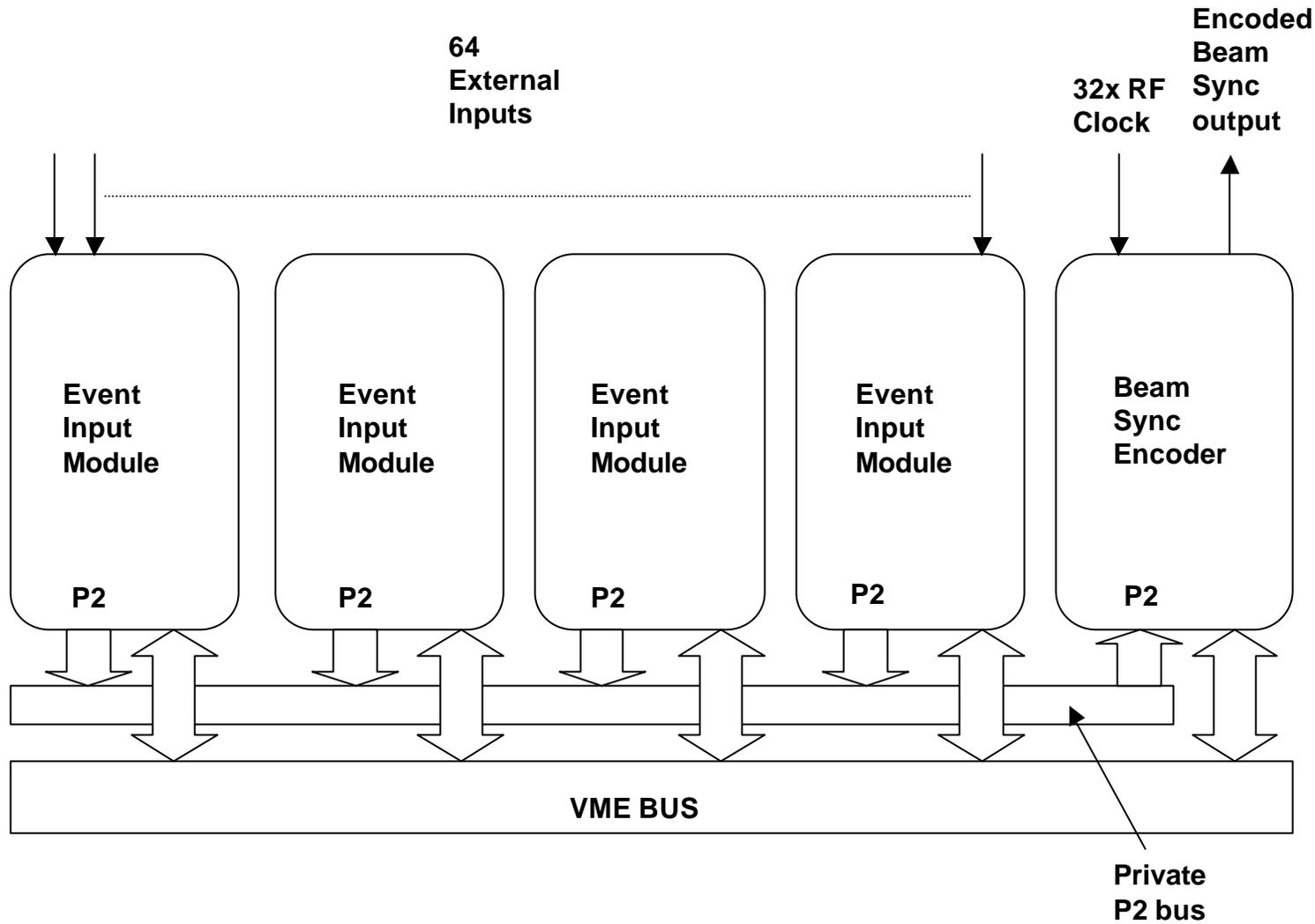
# H/W Components - Master

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- SNS Encoder
  - Prioritizes events
    - Hardware inputs have highest priority
    - Priority of hardware inputs position dependent
  - Remaining events 64 through 255 are provided via VME message stack
    - Message stack is sent during idle portion of cycle
  - Translation table maps hardware input to event code

# SNS Timing Encoder



# H/W Components - Decoder/Delay



- 1.19 MHz phased locked to the Beam Sync Clock carrier will be generated internally
- Programmable Event RAM
- Each channel comprises three cascaded delay stages:
  - Delay N beam revolutions (clocked by 1.19 MHz rotation clock)
  - Course phase delay ~52 ns steps
  - Fine phase delay
- Programmable pulse width

# H/W Components - Decoder/Delay



- Channel trigger source
  - Trigger on event(s)
  - Trigger on previous channel
- Inputs:
  - 19.02 MHz SNS clock
- Outputs:
  - 1.19 MHz RF clock
  - 19.02 MHz clock
  - output / delay channels (8)
  - Single ended TTL with 50 ohm drive capability

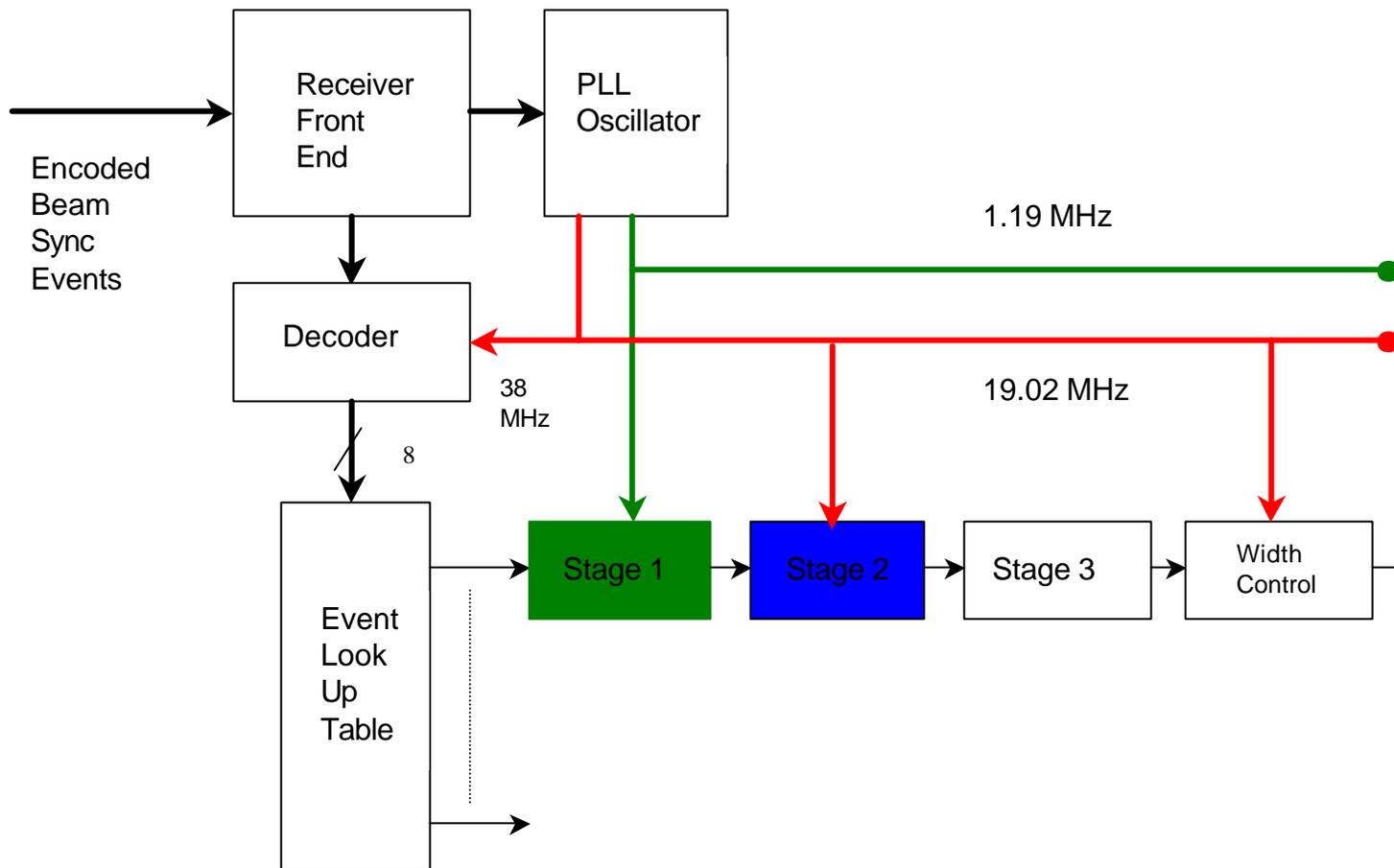
# H/W Components - Decoder/Delay

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- VME Interface
  - A16/D16
    - jumper selectable on 1K boundary
  - VME interrupt
    - Interrupt level and vector programmable
    - Link error
    - Terminal count

# Decoder Block Diagram



# Distribution



- Short Haul (< 300 ft)
  - Point to point shielded twisted pair
  - Inputs shall be transformer isolated
- Complimentary PECL
- Connector - Twinaxial BNC ??
  
- Long haul
  - Multimode fiber

# Schedule



- Design review by January/February 2000
- Detailed design begins Summer 2000

# Fermi Neutron Choppers



- Very high inertia rotors rotating at 600 RPS
- Synchronized to the 60 Hz powerline using DSP circuits & PLLs
- Neutron Choppers are synchronized to each other or a master chopper
- New systems expect to achieve  $1 \mu\text{s}$  between beam pulse and chopper

# Fermi Neutron Choppers



- Neutron chopper timing signal is used to control extraction from the accumulator ring
- Extraction timing accuracy needs to be  $\pm 1 \mu\text{s}$
- Extraction must be synchronized to the gap in the accumulated beam ( $\sim 280 \text{ ns}$  long)
- The rest of the facility is synchronized to meet this requirement