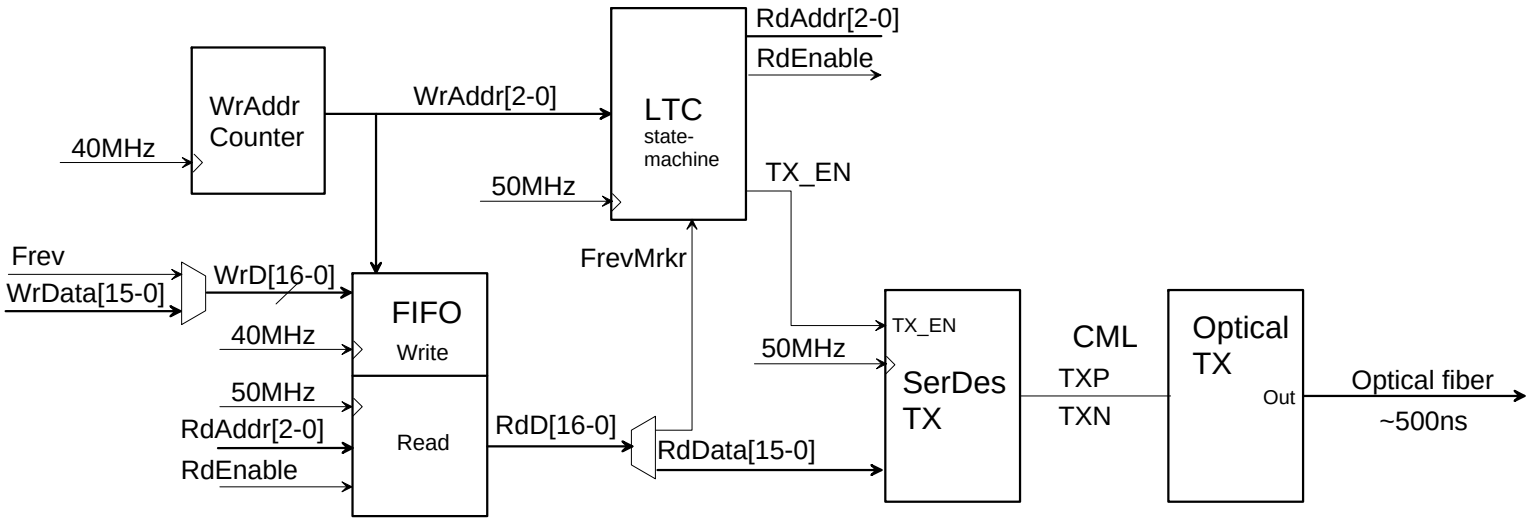
LHC Bunch Synchronous Digital Data Link

- Requirements
  - 40MSPS (bunch synch) over the 50MSPS (1Gbps) link
  - Automatic Link acquisition
  - Embedded means to transmit the bunch 1 reference
- Solution
  - Use Trx FiFo + pad 1 idle char (comma) when starving for data
  - Use Rx FiFo, start reading once almost filled
  - Once per machine turn (bunch 1 marker) insert a sequence of 4 successive commas
  - Detect a 4 comma reception in the Rx to determine the data phasing in respect to the machine turn.
  - The 4 comma sequence guarantees link acquisition

LHC Bunch Synchronous Digital Data Link

- Further Application
  - Easily add 1Turn circular DP memory at the Rx to create an exact 1T delay
    - Synchronize write address with comma burst detect
    - Synchronize read address with locally distributed Frev marker.

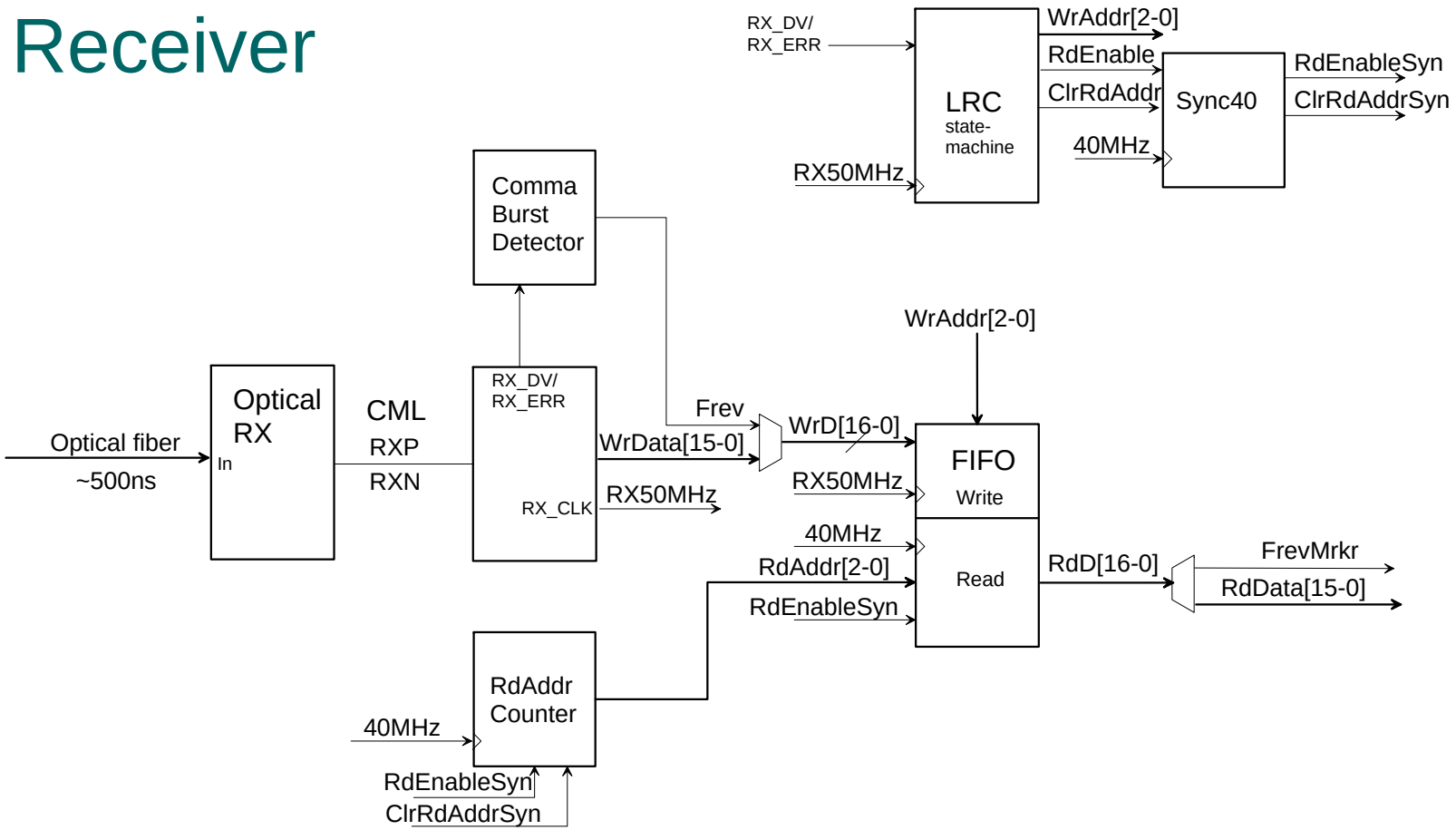
Transmitter



Overview

EDA-0xxxx	Title	Gigabit Link Transmitter Part	Page	1/1
	Designer	John C. Molendijk AB/RF/cs		
	Date	2006/01/12	Version	1.0

Receiver



Overview

EDA-0xxxx	Title	Gigabit Link Receiver Part	Page	1/1
	Designer	John C. Molendijk AB/RF/cs		
	Date	2006/01/12	Version	1.1