ILC LLRF Hardware Baseline

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Requirements for ILC

- CM energy: 500 GeV. Range 200 - 500 MeV. Upgradeability to 800 GeV
- Luminosity and reliability of the machine should allow L_{eq} = 500 fb^{-1} four years
- Energy scans between 200 GeV and 500 GeV. Energy change should take less than 10% of data taking time.
- Beam energy stability and precision should be below the tenth of percent level

Requirements for Main Linac

	phase tolerance limiting luminosity loss (deg)	phase tol. limiting incr. in energy spread (deg)	amplitude tolerance limiting luminosity loss (%)	amplitude tolerance limiting increase in energy spread (%)
correlated BC phase errors	.24	.35		
uncorrelated BC phase errors	.48	.59		
correlated BC amplitude errors			0.5	1.8
uncorrelated BC amplitude errors			1.6	2.8
correlated linac phase errors	large	.36		
uncorrelated linac phase errors	large	5.6		
correlated linac amplitude errors			large	.07
Uncorr. linac amplitude errors			large	1.05

Summary of tolerances for phase and amplitude control. These tolerances limit the average luminosity loss to <2% and limit the increase in RMS center-of-mass energy spread to <10% of the nominal energy spread.

Ref. Mike Church

Scope of Main Linac LLRF

total number of klystrons / cavities per linac	~ 350/ 8,400
per rf station (klystron):	
# cavities / 10 MW klystron	~ 26
# of precision vector receivers (probe, forward, reflected power, reference line, beam)	~90
# piezo actuator drivers / motor tuners	~ 26/26
# waveguide tuner motor controllers	~ 26
# vector-modulators for klystron drive	1
Total # of meas. / control channels per linac	~30,000 / ~30,000

Requirements

- **Reliability**
  - *not more than 1 LLRF system failure / week*
  - *minimize LLRF induced accelerator downtime*
  - *Redundancy of LLRF subsystems*
  - *…*
- **Operability**
  - *"One Button" operation (State Machine)*
  - *Momentum Management system*
  - *Automated calibration of vector-sum*
  - *…*
- **Reproducible**
  - *Restore beam parameters after shutdown or interlock trip*
  - *Recover LLRF state after maintenance work*
  - *…*

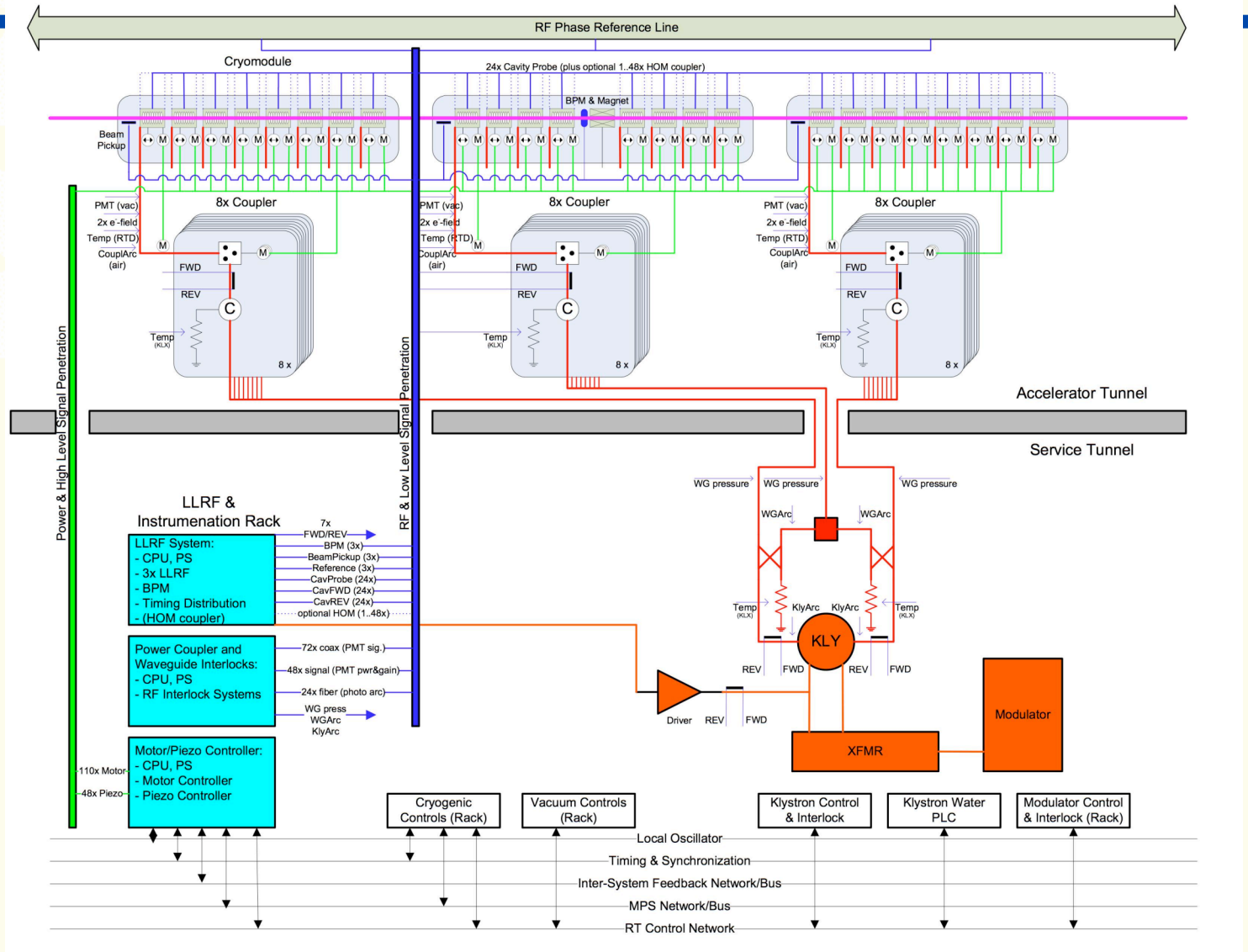
Requirements

- Maintainable
  - *Remote diagnostics of subsystem failure*
  - *"Hot Swap" Capability*
  - *Accessible Hardware*
  - *...*
- **Well Understood**
  - *Performance limitations of LLRF fully modelled*
  - *No unexpected "features"*
  - *...*
- **Meet (technical) performance goals**
  - *Maintain accelerating fields - defined as vector-sum of 24 cavities - within given tolerances*
  - *Minimize peak power requirements*
  - *...*

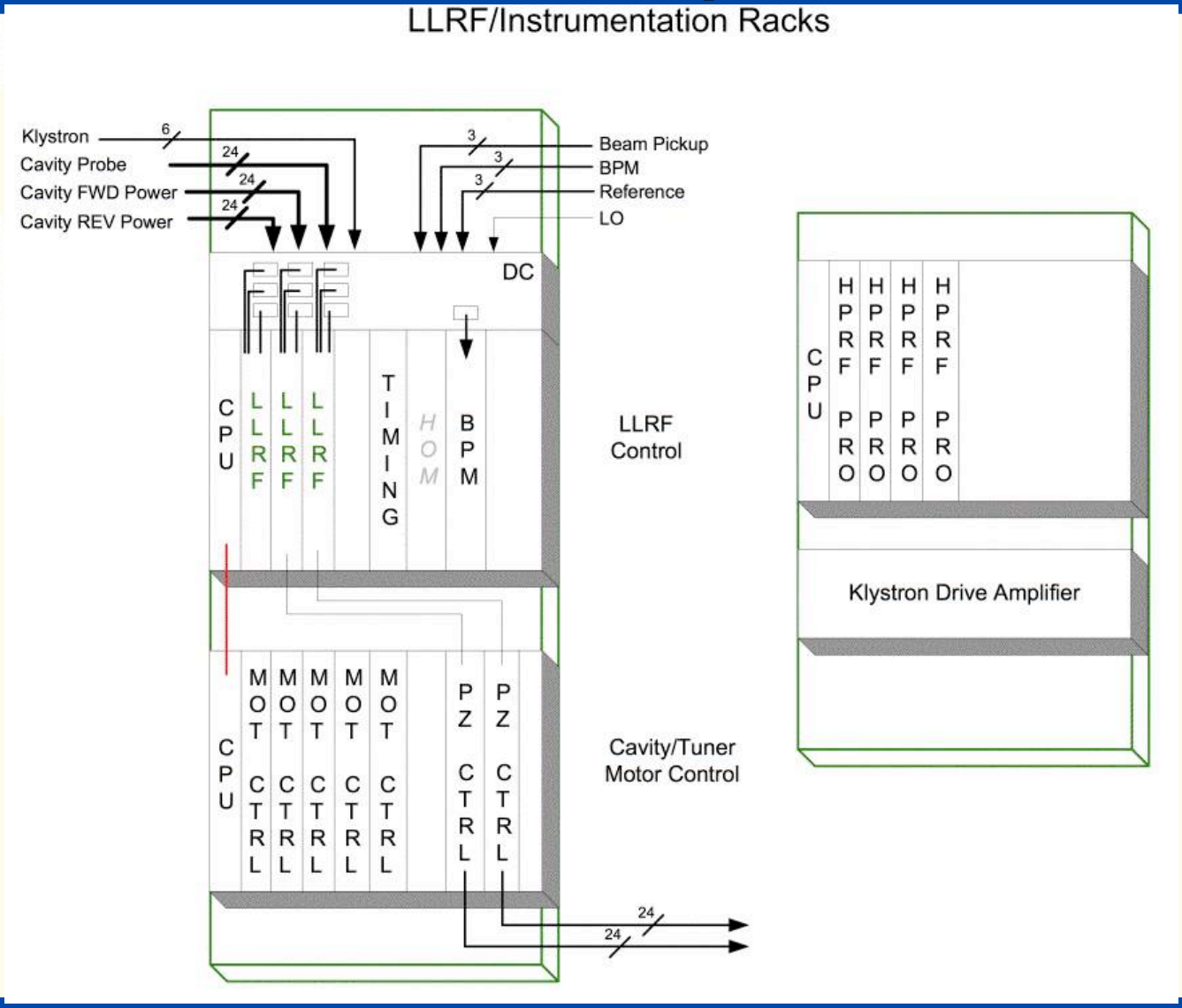
Current ILC LLRF Baseline

- Serves as a Costing Model
- We are converging on a general architecture yet remain open to innovation
- Each of the three regions are currently exploring designs that will be installed in their own test strings.
- Due to the large number of stations in the Main Linac and the tight specifications in the crab cavities and Buncher sections, the final accelerator may have multiple designs.
- Final architecture for the ML should converge by the completion of the EDR.
- Common elements to the 3 regions designs are:
  - Crate based modular electronics
  - CPU for local computation and control interface
  - FPGA for low latency processing backed up with DSP

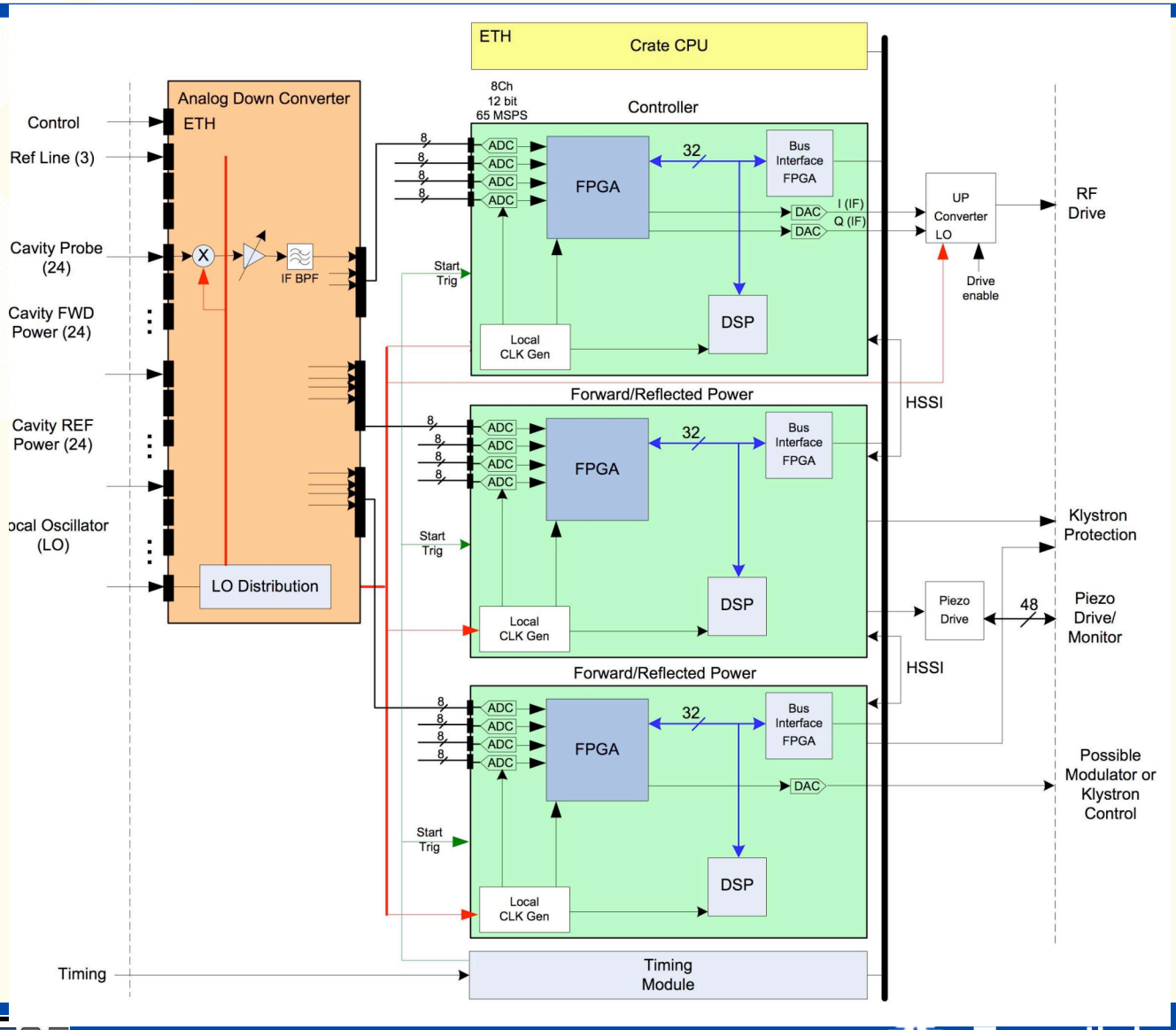
RF Station with 3 Cryomodules



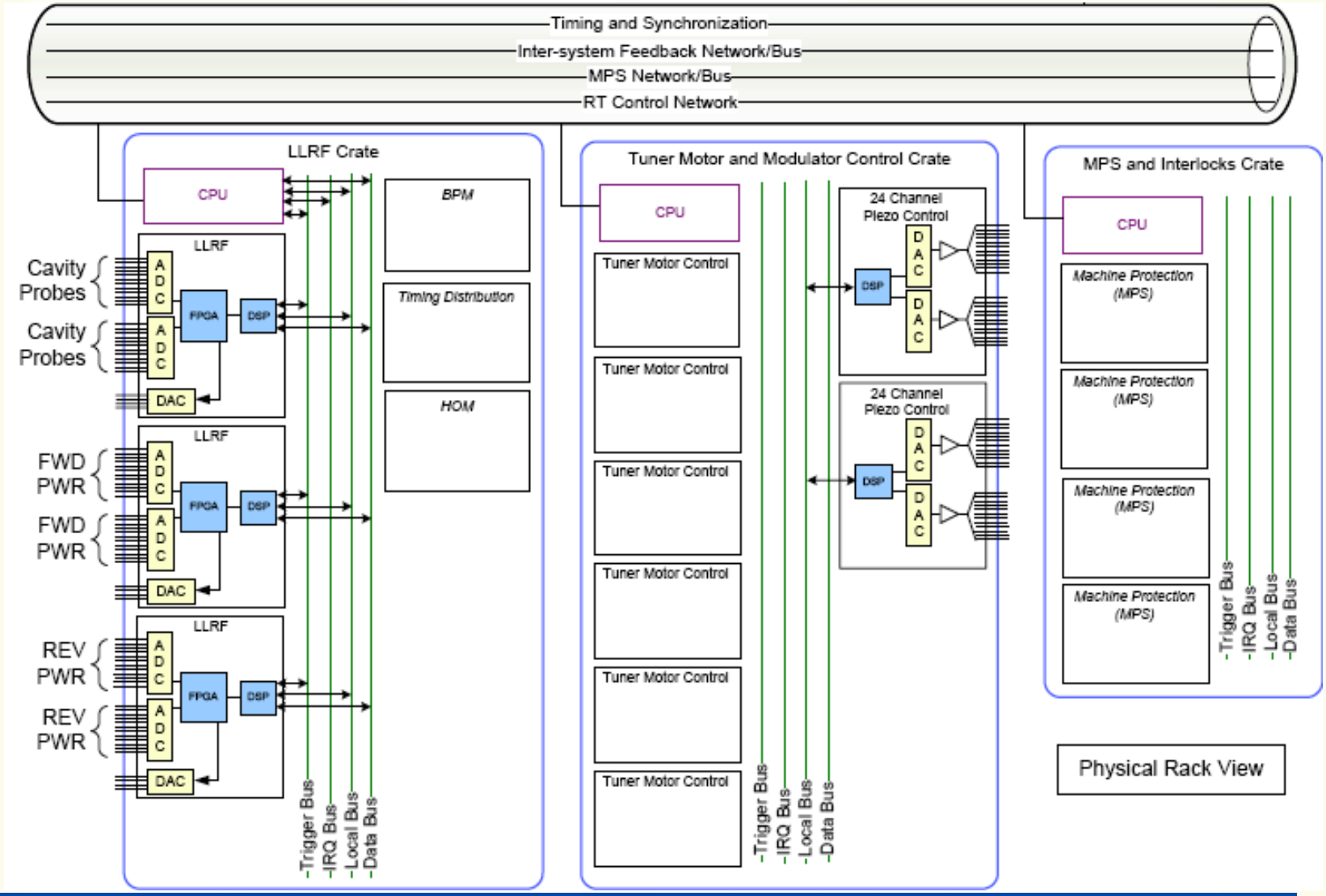
Rack Layout


LLRF/Instrumentation Racks
Klystron
Cavity Probe
Cavity FWD Power
Cavity REV Power
6
24
24
24
3
3
3
Beam Pickup
BPM
Reference
LO
DC
CPU
LLRF
LLRF
LLRF
TIMING
HOM
BPM
LLRF Control
CPU
MOT CTRL
MOT CTRL
MOT CTRL
MOT CTRL
MOT CTRL
PZ CTRL
PZ CTRL
Cavity/Tuner Motor Control
24
24
CPU
HPRF PRO
HPRF PRO
HPRF PRO
HPRF PRO
Klystron Drive Amplifier

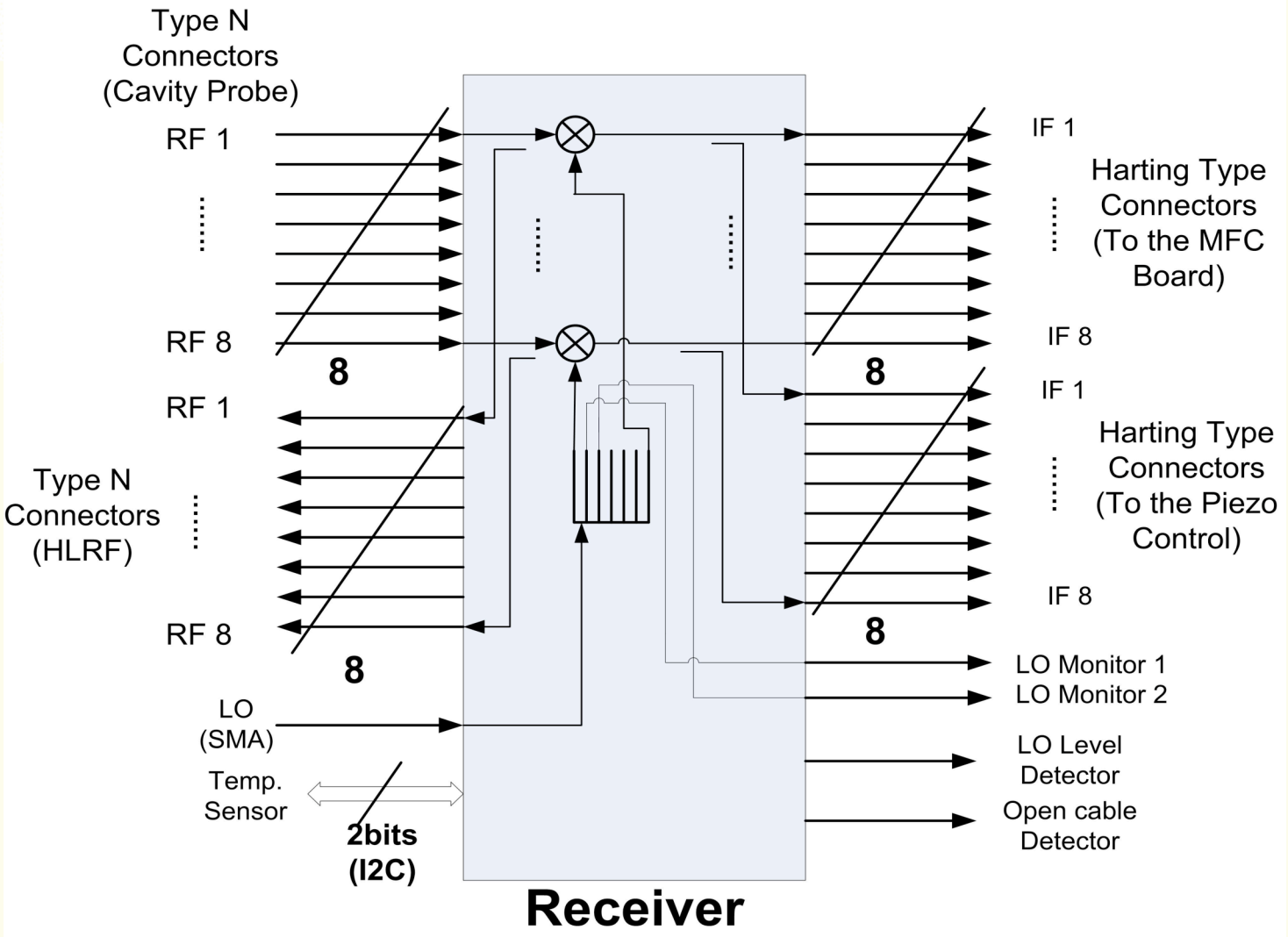
LLRF Rack Detail



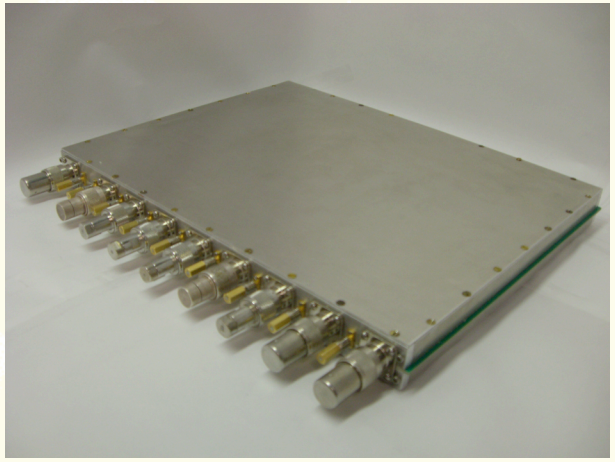
LLRF Crate Detail

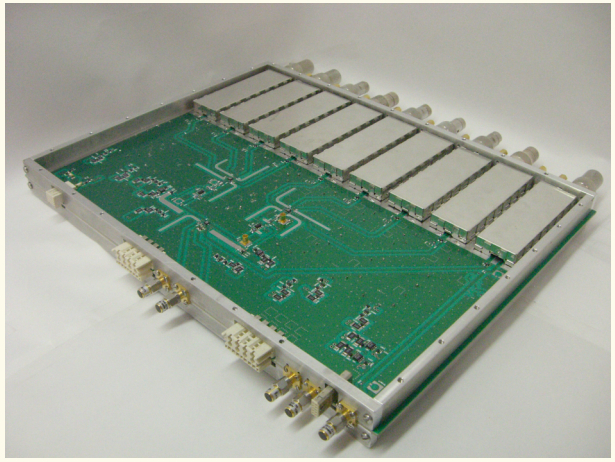


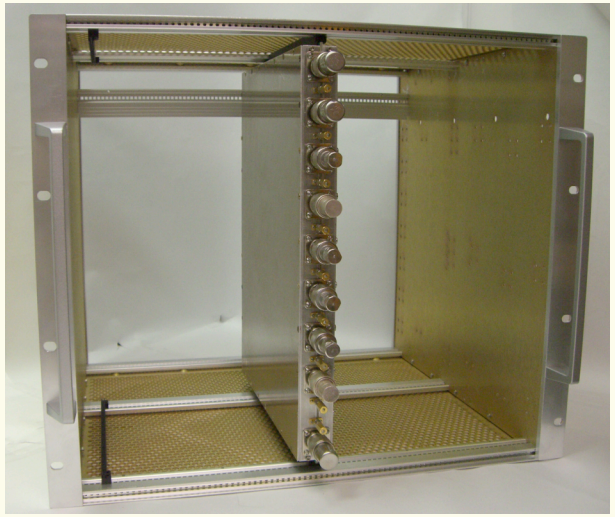
Receiver Section

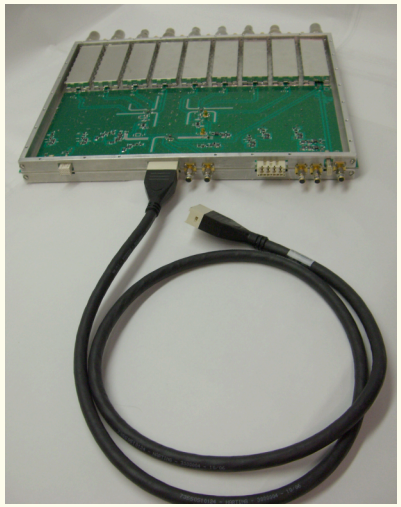


Pictures of the Receiver

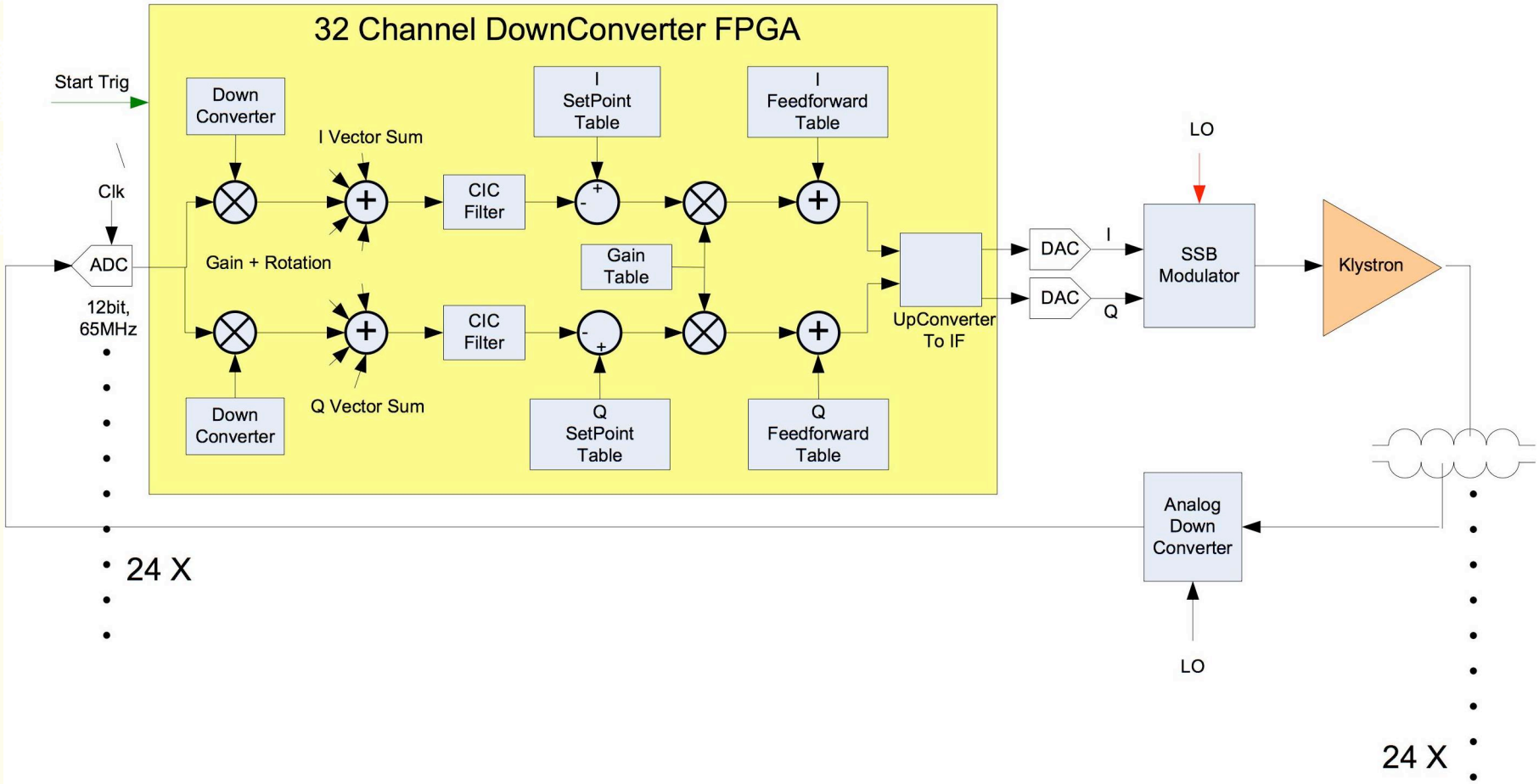




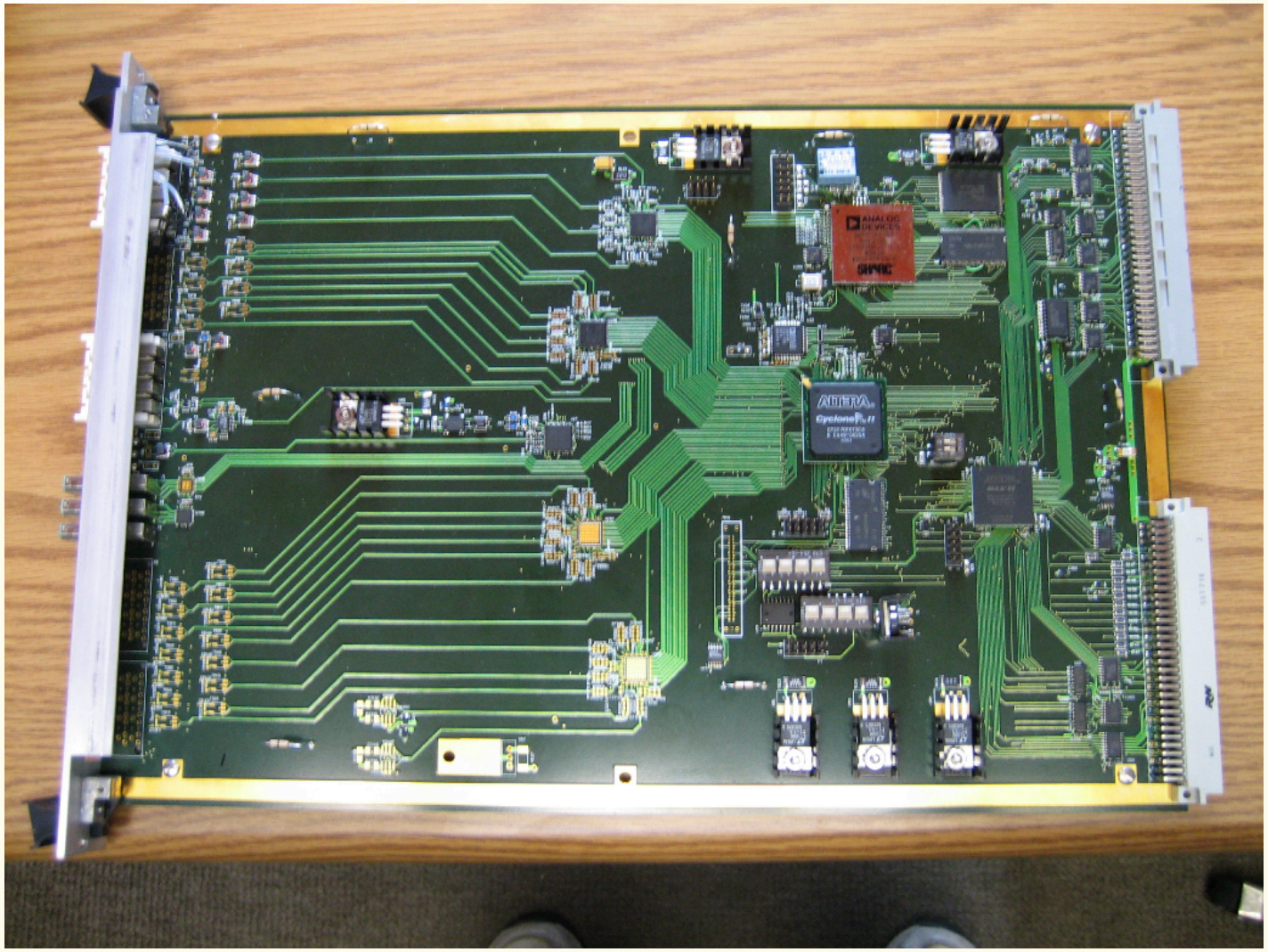




Simplified Controller Diagram



33 Channel MFC Board



Channel Average Gain for 8 Channels

8 Channel Rx
And MFC

Measured SNR for one channel

(12bit ADC):

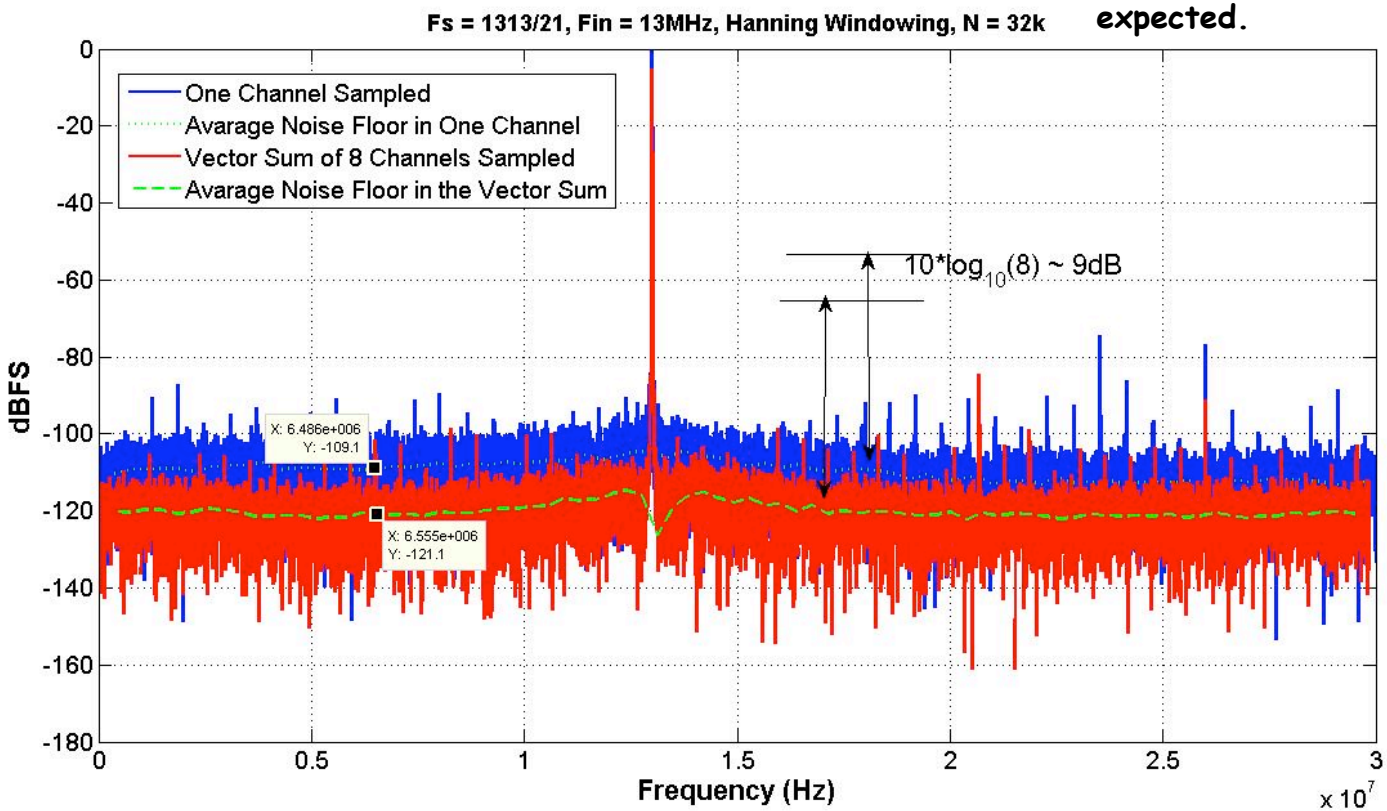
SNR@fs/2 = 112dB - 10log$_{10}$(32k/2) = 70dB

Measured SNR for vector sum

(8x12bit ADC):

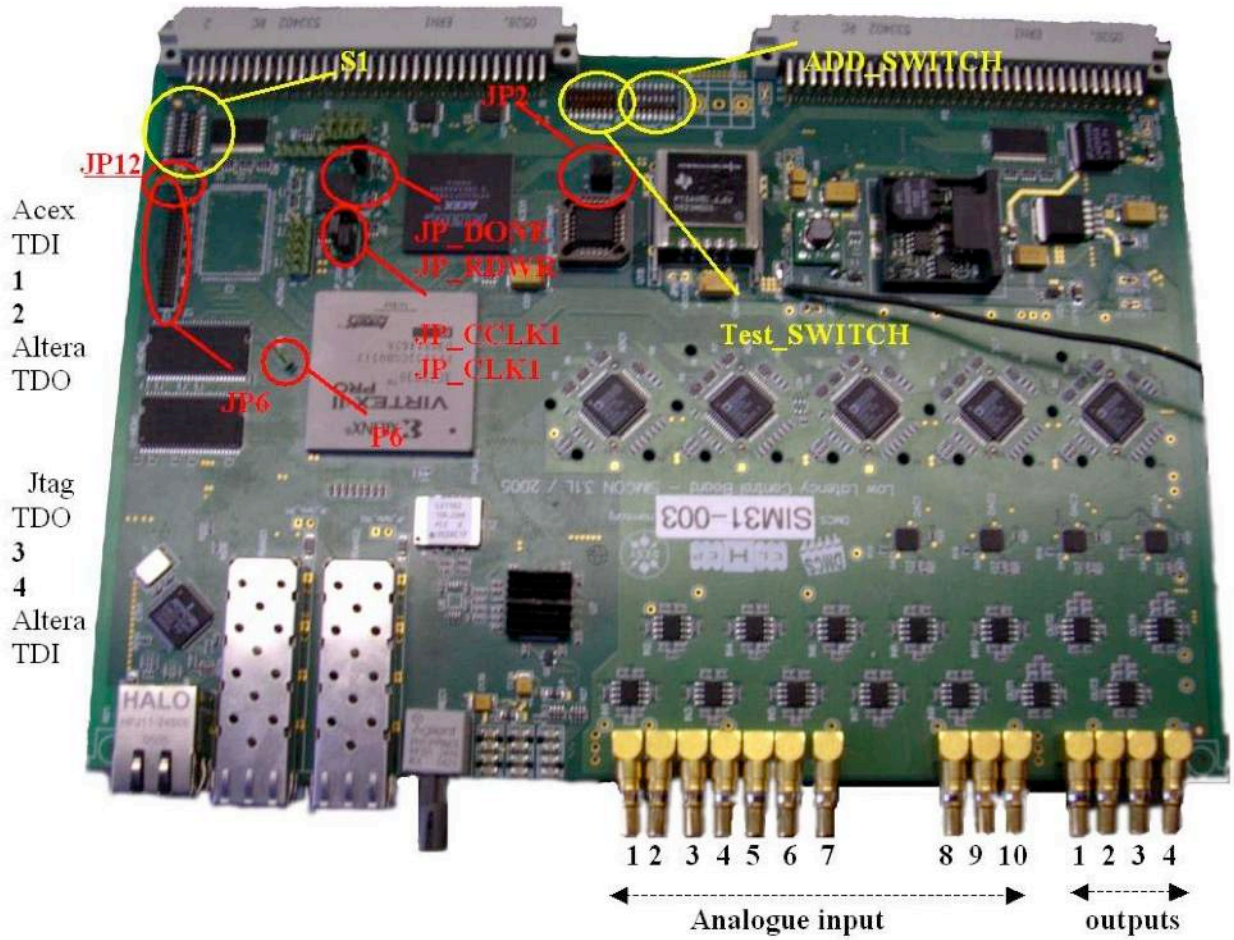
SNR@fs/2 + 10log$_{10}$(8) = 79dB

The SNR -156dBc/Hz (0.0016% BW:1MHz) is expected.



DESY SIMCON3.1 Controller

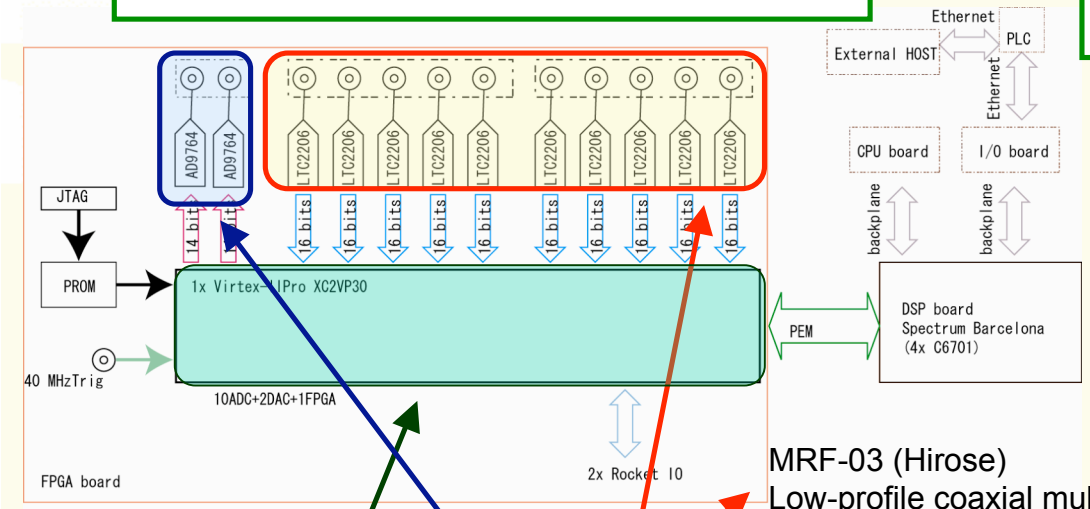
2.SIMCON3.1 board description and schematics.



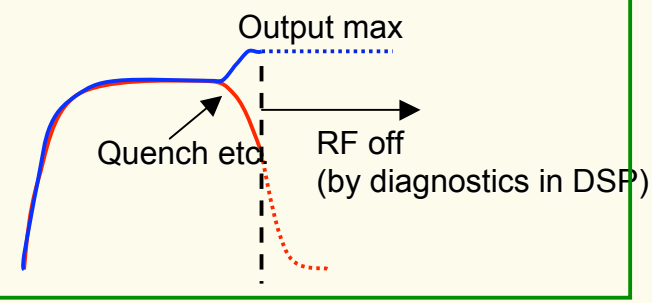
FPGA & DSP boards @STF Phase1

Custom FPGA board
: Mezzanine card of the commercial DSP board
10 **16bit-ADCs** and 2DACs + 2Rocket IO
40 MHz clock

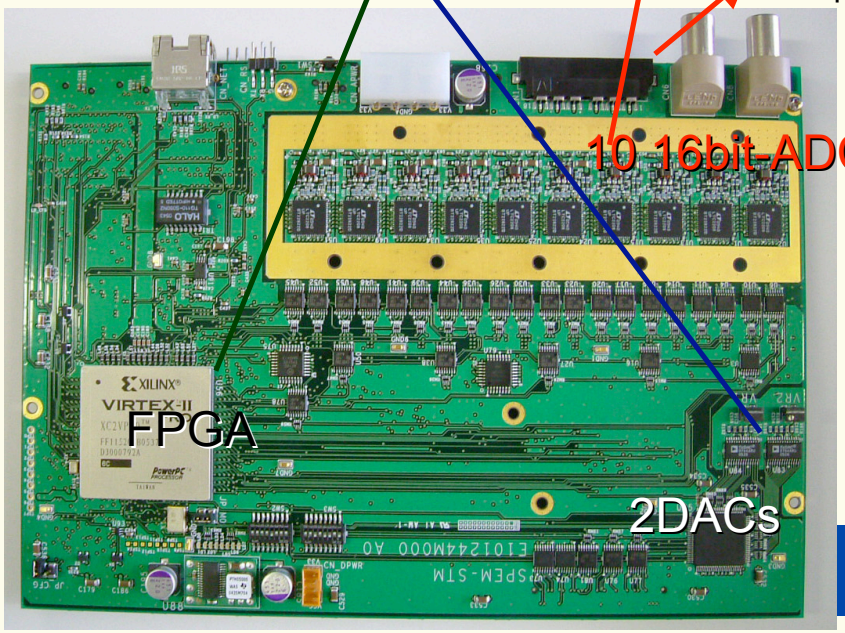
Commercial DSP board (Barcelona)
(same to J-PARC system)
:4x TI C6701 DSPs
Can access to FPGA like an external memory of DSP

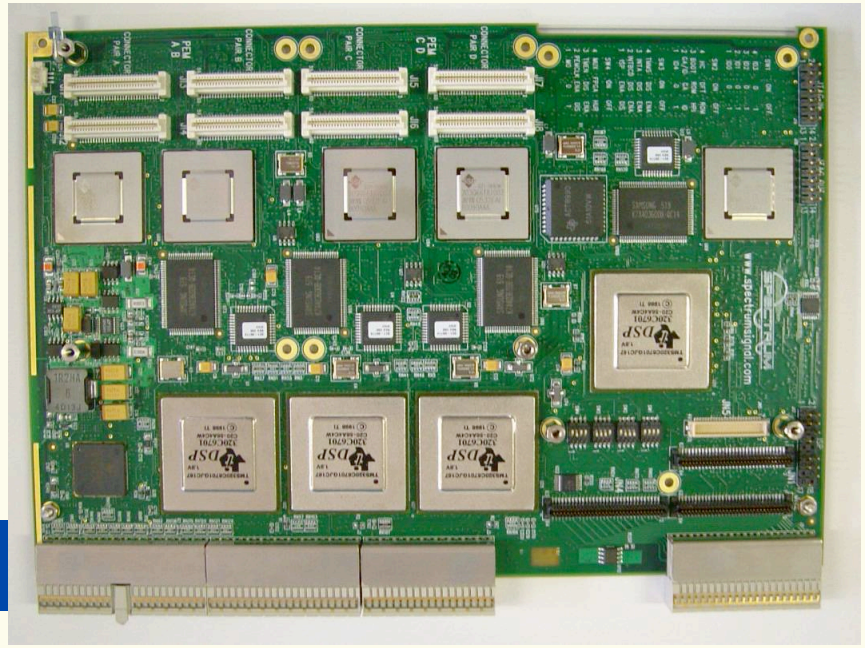


Real time intelligent diagnostics by DSP board



MRF-03 (Hirose)
Low-profile coaxial multiple contact connector





Design Goals for Cost Reduction

- Reduce the heat load
  - Power off circuits between pulses
  - If the heat load is low enough then we may eliminate the expensive water cooled rack
- Evaluate crate standards and need for CPU
- Simplify process chain for forward and reflected power
- Experiment with smaller, cheaper coax
- Evaluate downconverters in accelerating tunnel.