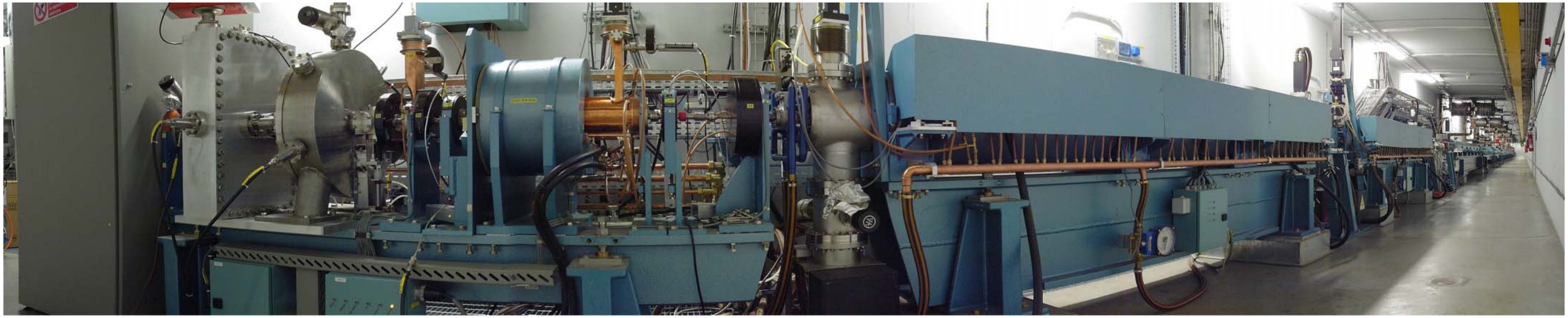
The FERMI LLRF System

(and a method for controlling distortion)

Tony Rohlev Larry Doolittle



Knoxville October 23, 2007

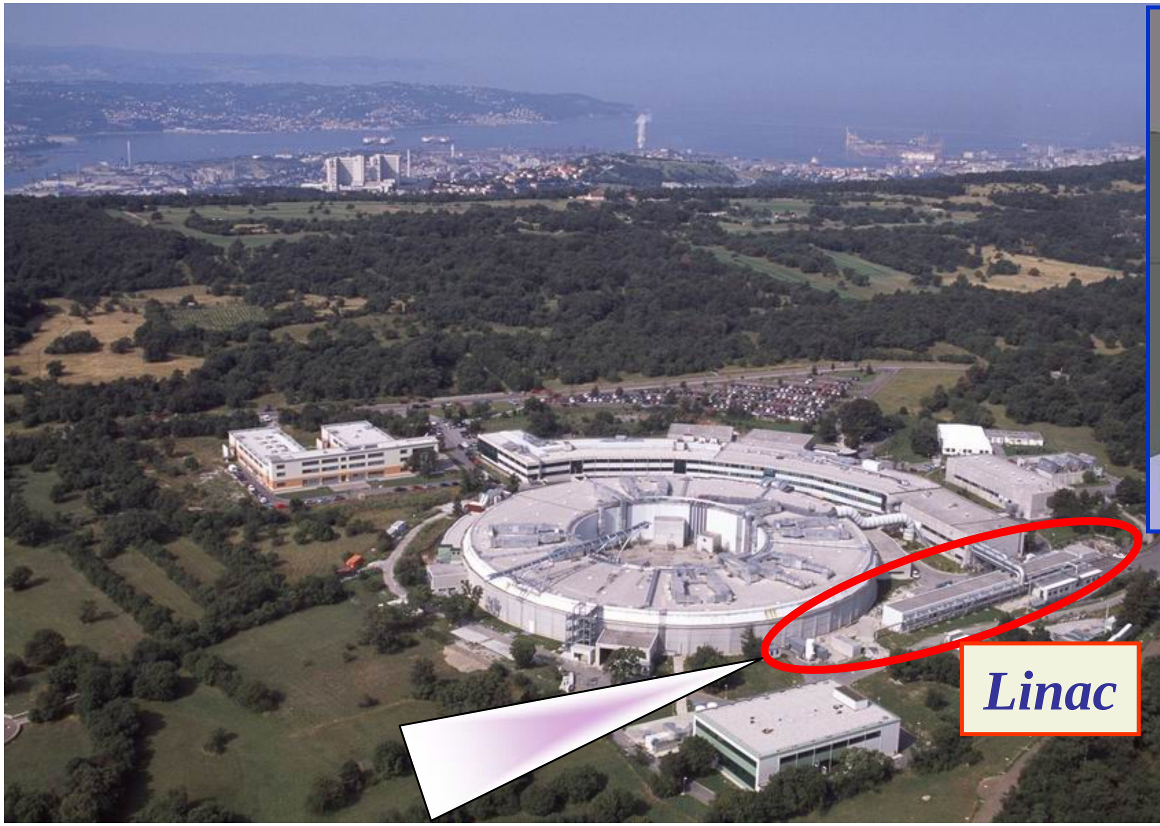
Outline

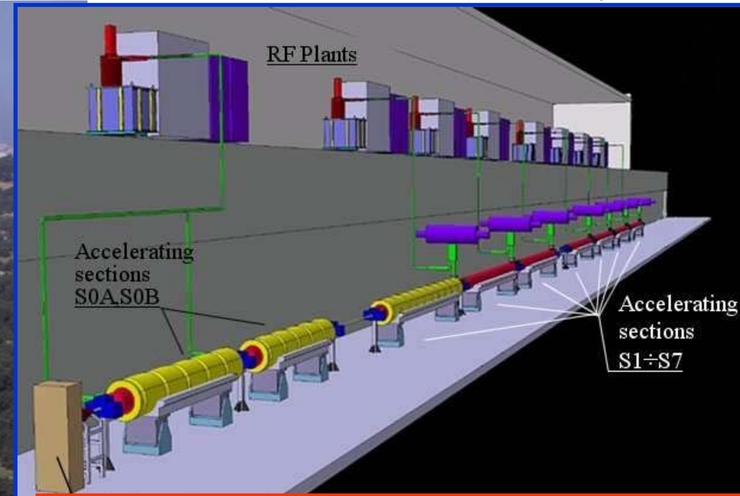
- ***The FERMI Linac** (with its intolerant tolerances)*
- ***The proposed FLLRF system** (full of tricks, new and old)*
- ***Correcting hardware with software** (one such trick)*

The Fermi FEL Linac

- Development of a single-pass FEL User Facility based on the existing Normal Conducting S-band Linac.
- Fixed beam energy (1.2 GeV), 50 Hz pulse rep. rate, 1 e-bunch/pulse.
- Seeded operation with Harmonic Generation.
- Spectral range:
  - Phase I 100 – 40 nm, single stage FEL-1
  - Phase II 40 – 10 nm, two stages FEL-2
- Short sub-ps pulses ≤ 200 fs, and long pulses, up to 1.4 ps (flat part).
- Flexible polarization, gap tuning, apple type undulators.

	Medium pulse	*Long pulse*	
Electron beam *parameter*	***Value***		***Units***
Beam energy	1.2		GeV
Peak current	800	500	A
Extracted charge	0.3	1.0	nC
Uncorrelated energy spread	≤ 200		KeV
Normalized emittance (slice)	≤ 1.5		mm mrad
Bunch length	0.7	up to 1.4	ps

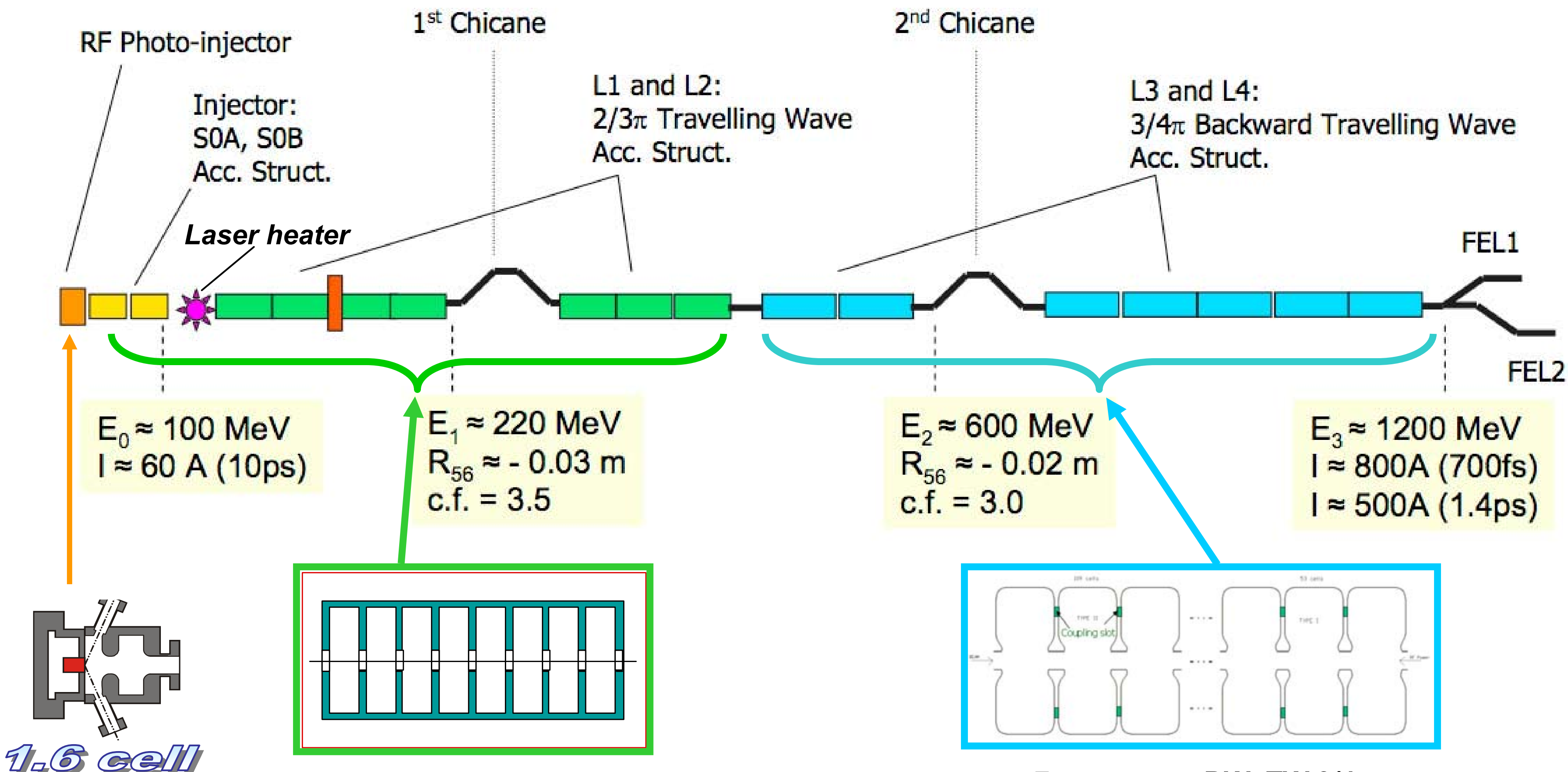




Available:

- **8 Klystron stations;**
- **9 Accelerating sections:**
  - **2 FW_TW 3 m**
  - **7 BW_TW 6 m**
- **7 Accelerating sections donated by CERN.**

Machine layout

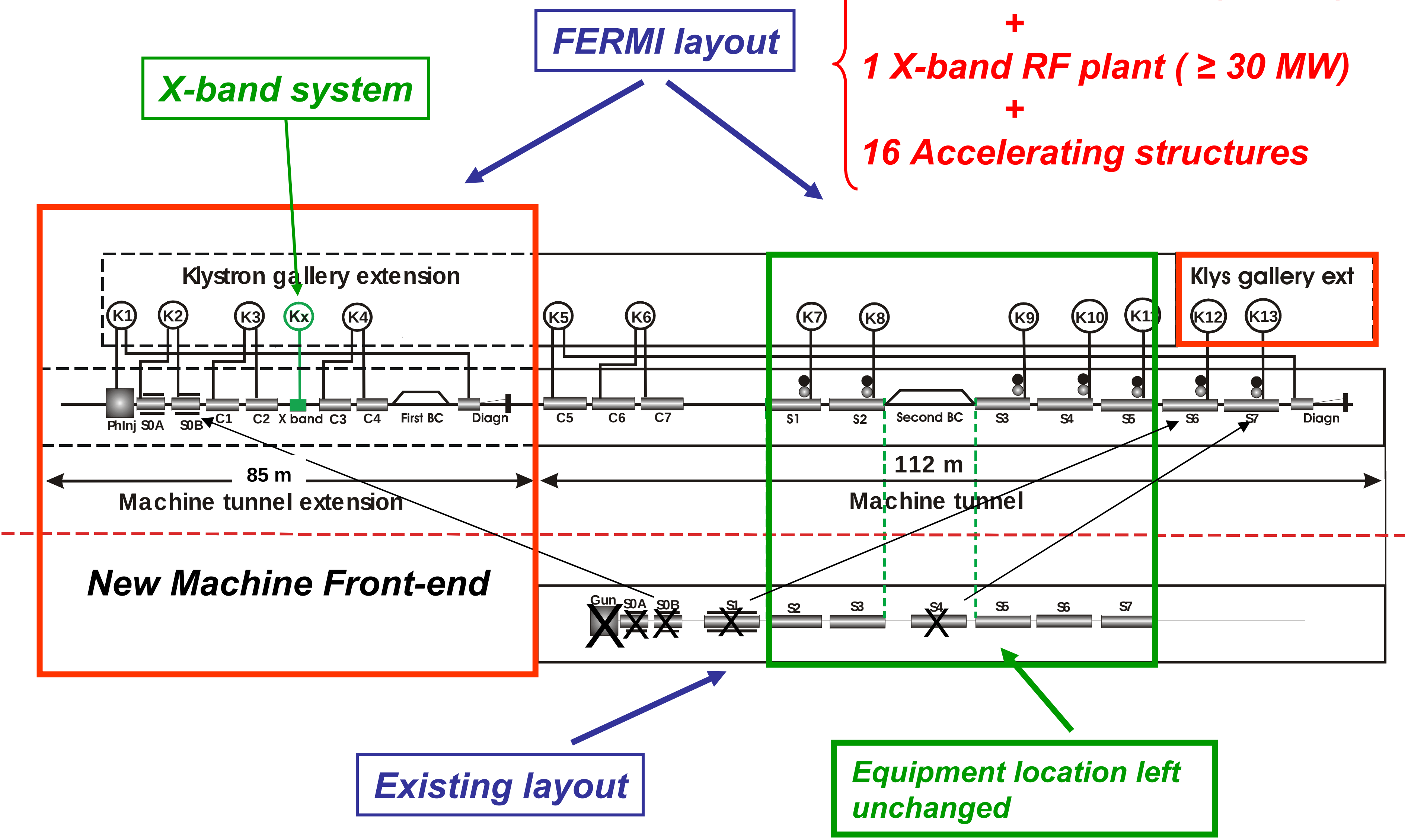


9 Slac type FW_TW 2/3 π
(3.0 - 4.5 m) without Sled

7 nose cone BW_TW 3/4 π
(6.1 m) with Sled

RF Plants

14 S-band RF plants (45 MW)
+
1 X-band RF plant (≥ 30 MW)
+
16 Accelerating structures



- Linac: NC, pulsed @ 50 Hz, 150 meters long
- RF Plants: 15 total (7 @ 2 cav/kly, 8 @ 1 cav/kly)
- Beam: e^-, 800 A pk, <1.4 ps long, 1 bunch/pulse, so: essentially invisible to LLRF system
- RF: 4.5 μs pulses, 800 to 1200 ns fill time for S structures, 100ns fill time for X structure
- Transport delay: 95 ns for single cavity, 150 ns for dual (rt)
- Control type: Feed-forward (open-loop) for each pulse Feedback (adaptive learning) pulse to pulse PtP

Sensitivities and tolerance budget for long pulse

Using the tolerance budgets in table all of the requirements will be met at the same time:

$|\Delta I/I0|<10\%$ $|\Delta E/E0|<0.1\%$ $|\Delta t|<150fsec$

(RMS values)

Tolerance budgets

There are three possible tolerance budgets. If the smaller tolerance from each column is applied (bold-type) all requirements will be met in the same time.

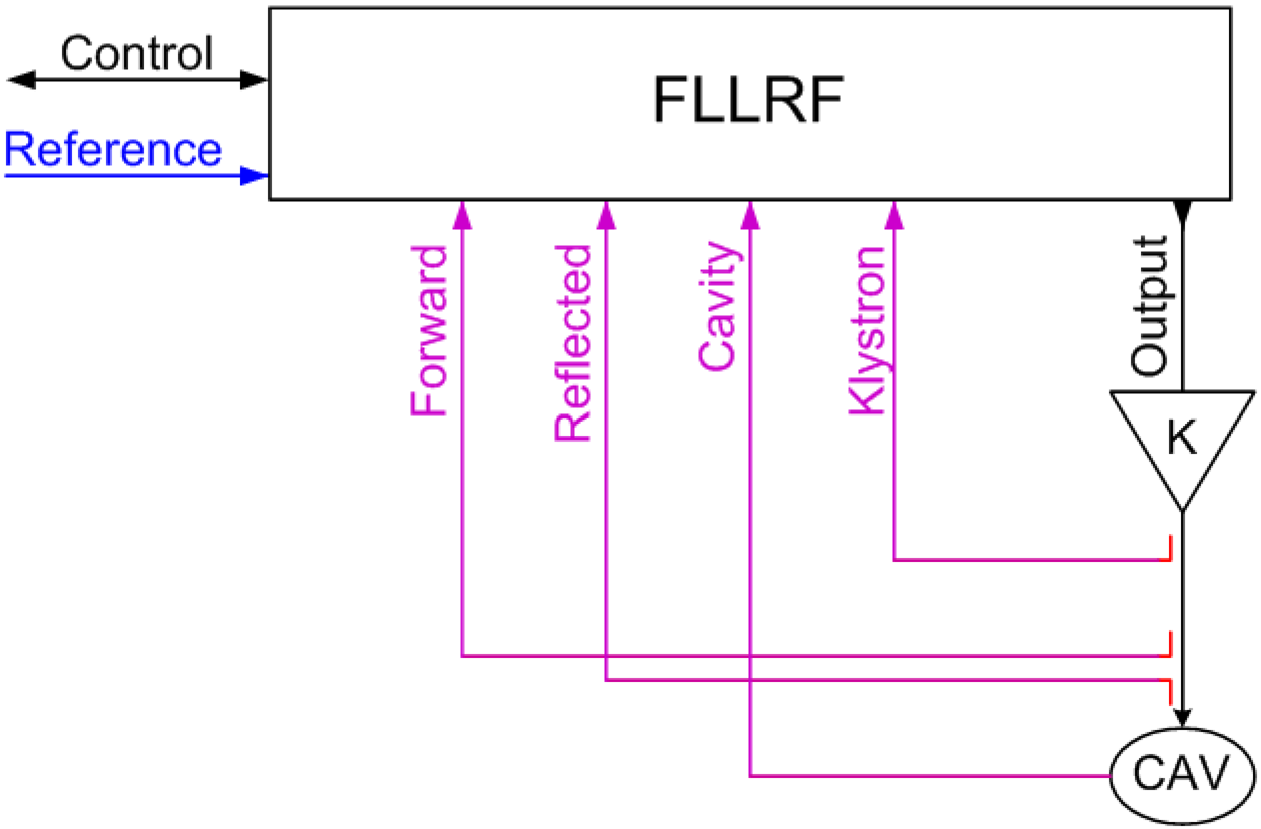
Parameter	Sy.	Unit	p_{sen} $\lvert\Delta I/I_0\rvert=10\%$	p_{sen} $\lvert\Delta E/E_0\rvert=0.1\%$	p_{sen} $\lvert\Delta t\rvert=150fsec$	p_{tol} $\lvert\Delta I/I_0\rvert<10\%$	p_{tol} $\lvert\Delta E/E_0\rvert<0.1\%$	p_{tol} $\lvert\Delta t\rvert<150fsec$
C1-C4 RF phase (L1)	$\varphi 1$	deg	**0.27**	0.60	0.14	0.15	0.20	**0.09**
X band phase (LX)	φx	deg	2.57	5.35	1.74	**0.30**	**0.30**	**0.30**
C5-C7 RF phase (L2)	$\varphi 2$	deg	3.09	3.51	3.12	0.30	**0.20**	0.30
S1-S2 RF phase (L3)	$\varphi 3$	deg	1.46	0.92	0.67	0.30	0.20	**0.15**
S3-S7 RF phase (L4)	$\varphi 4$	deg	>20	3.04	>20	3.00	**0.15**	1.00
C1-C4 RF voltage (L1)	$\Delta V_1/V_1$	%	1.38	2.19	0.21	0.30	0.25	**0.10**
X band voltage (LX)	$\Delta Vx/Vx$	%	4.49	24.59	3.35	0.60	**0.50**	**0.50**
C5-C7 RF voltage (L2)	$\Delta V_2/V_2$	%	7.82	0.82	0.52	1.00	0.15	**0.12**
S1-S2 RF voltage (L3)	$\Delta V_3/V_3$	%	6.16	0.50	0.31	1.00	**0.10**	**0.10**
S3-S7 RF voltage (L4)	$\Delta V_4/V_4$	%	>20	0.20	>20	4.00	**0.08**	0.40
Gun timing jitter	Δt_0	psec	0.93	0.49	3.10	0.50	**0.30**	0.35
Initial bunch charge	$\Delta Q/Q$	%	32.25	10.31	9.71	10.00	4.00	**3.00**

The sensitivities are used to generate a tolerance budget based on summing random, uncorrelated effects:

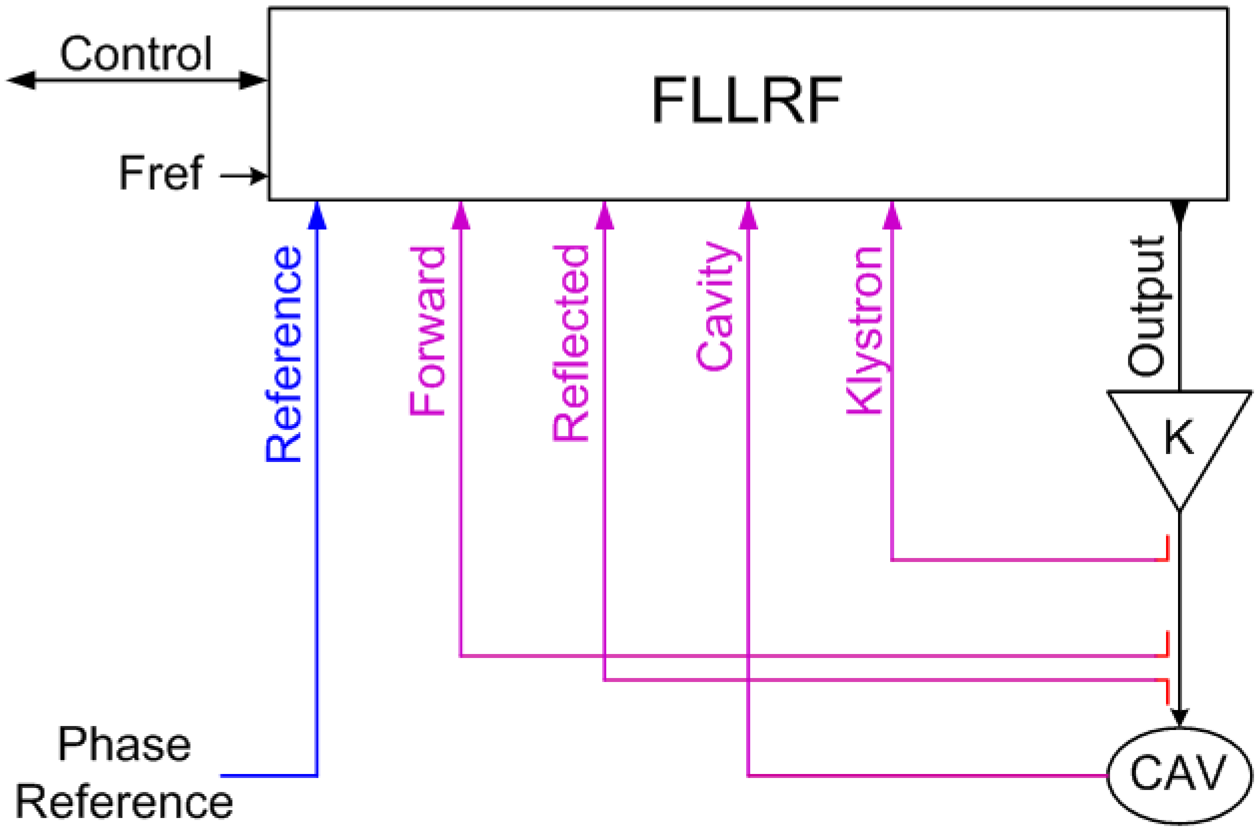
$$\sqrt{\sum_{i=1}^{N}\left(\frac{p_{tol}}{p_{sen}}\right)_i^2}<1$$

The tolerance, for each parameters, are p_{tol} while p_{sen} are weighting value in the summation. If the tolerances are chosen such that, $p_{tol} < p_{sen}$ for all i, a budget is formed.

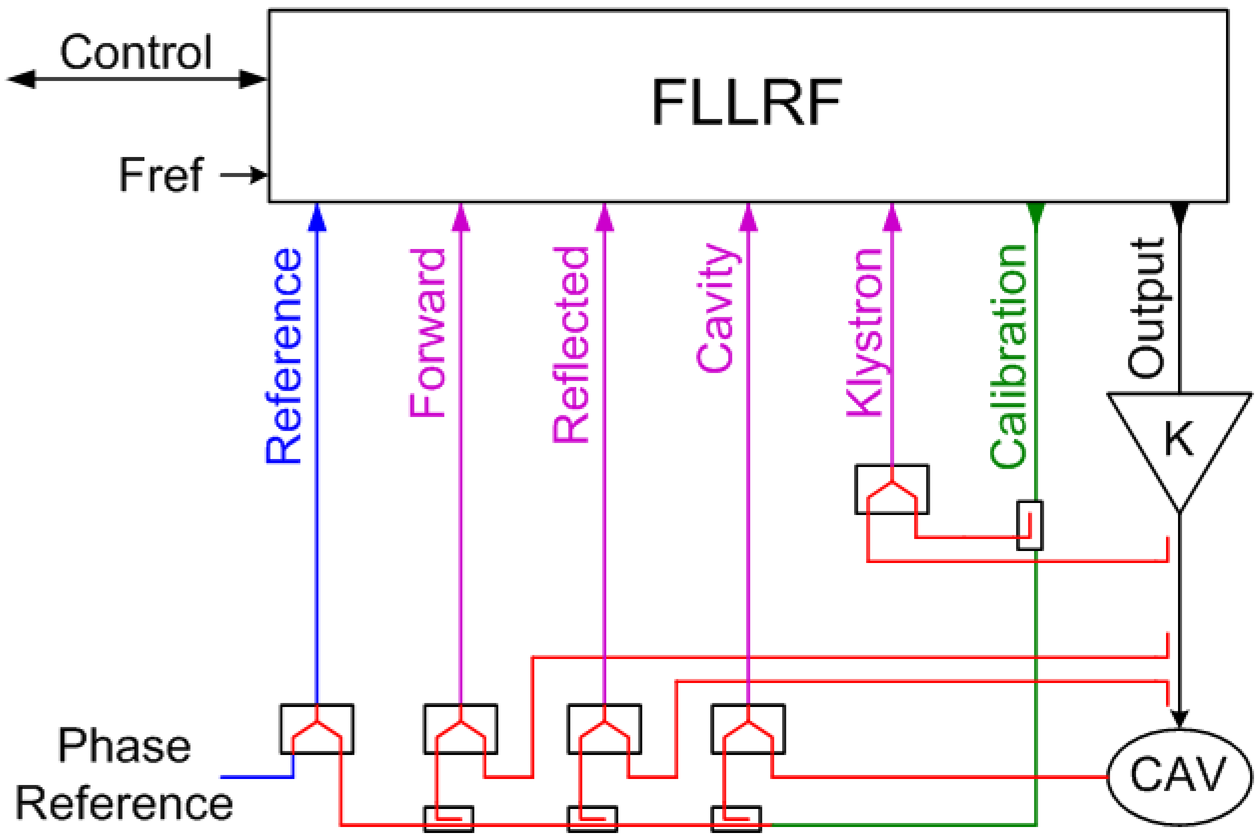
By P. Craievich 29.03.06


Control
Reference
FLLRF
Forward
Reflected
Cavity
Klystron
Output
K
CAV

FLLRF Layout with Reference as Input

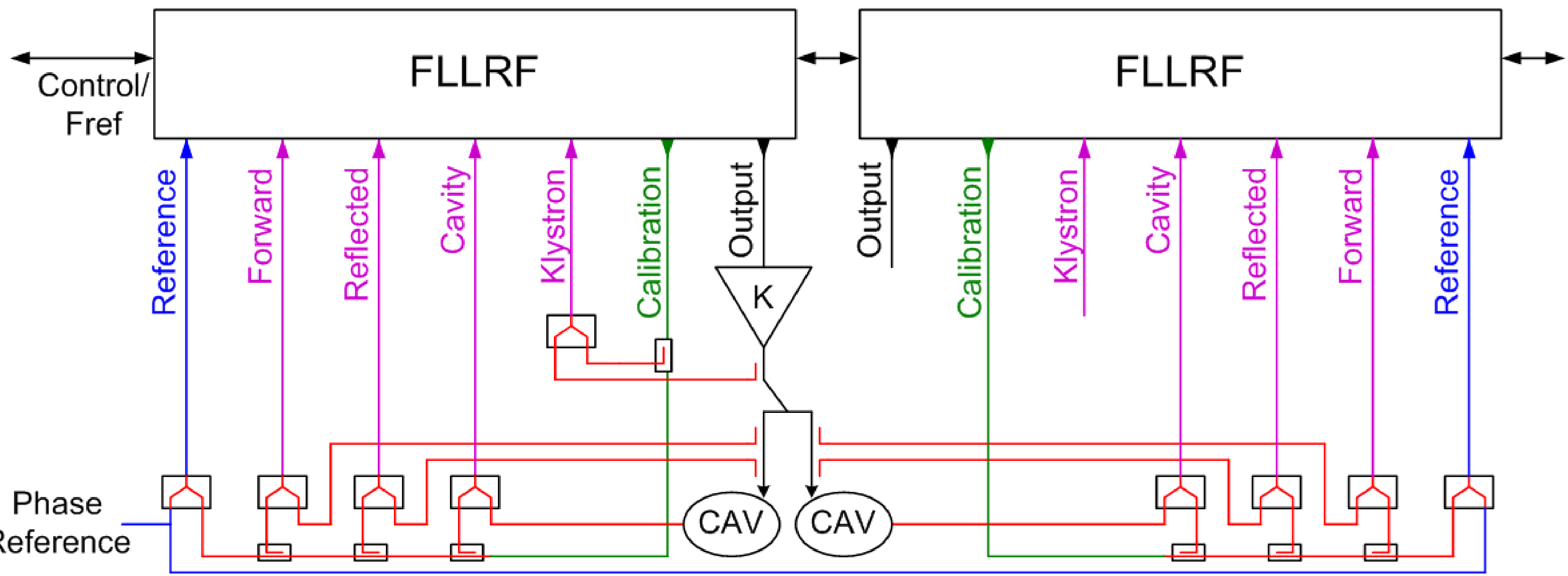


FLLRF Layout with Calibration Output



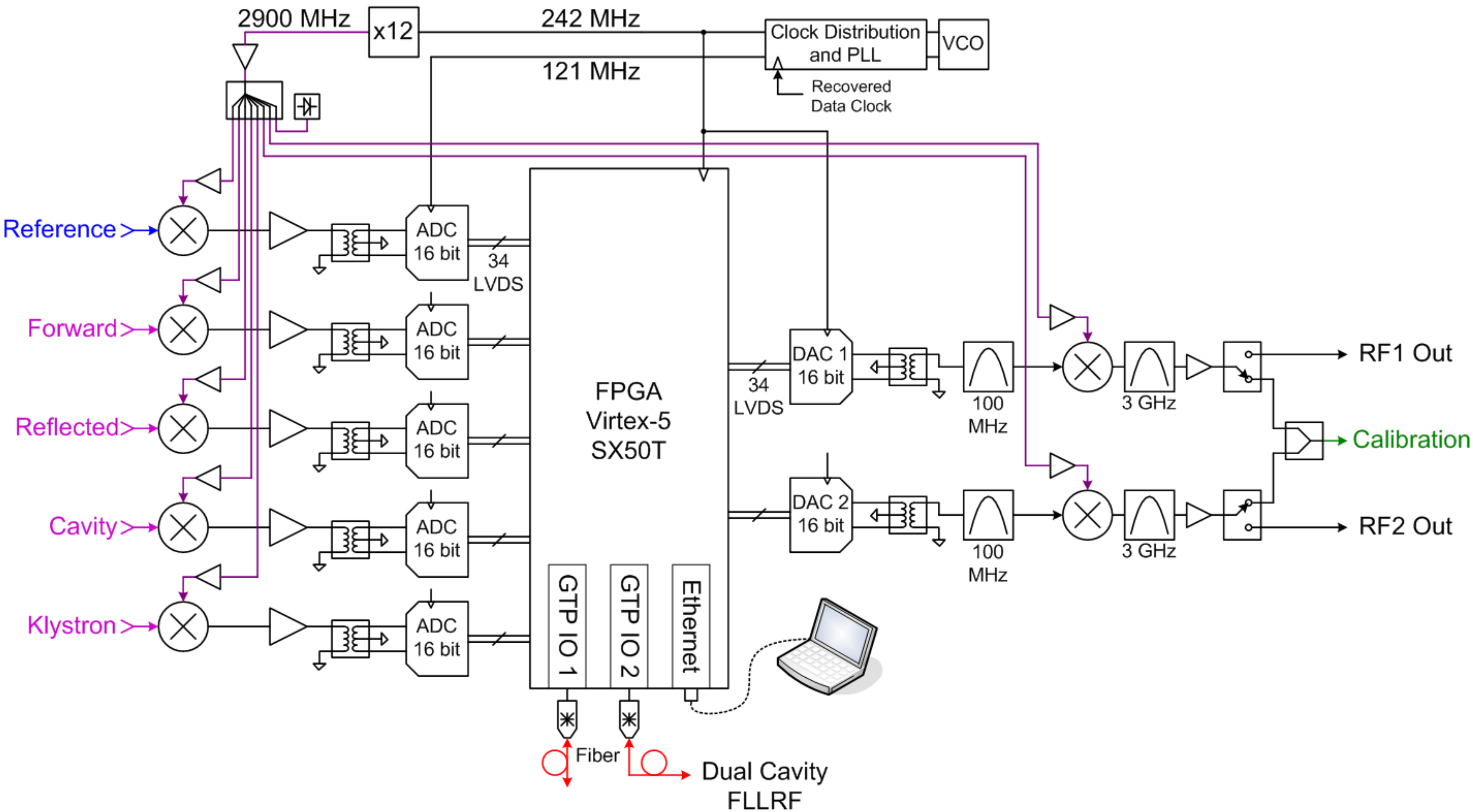
Red lines can not be actively calibrated

FLLRF Layout for Dual Cavity Control

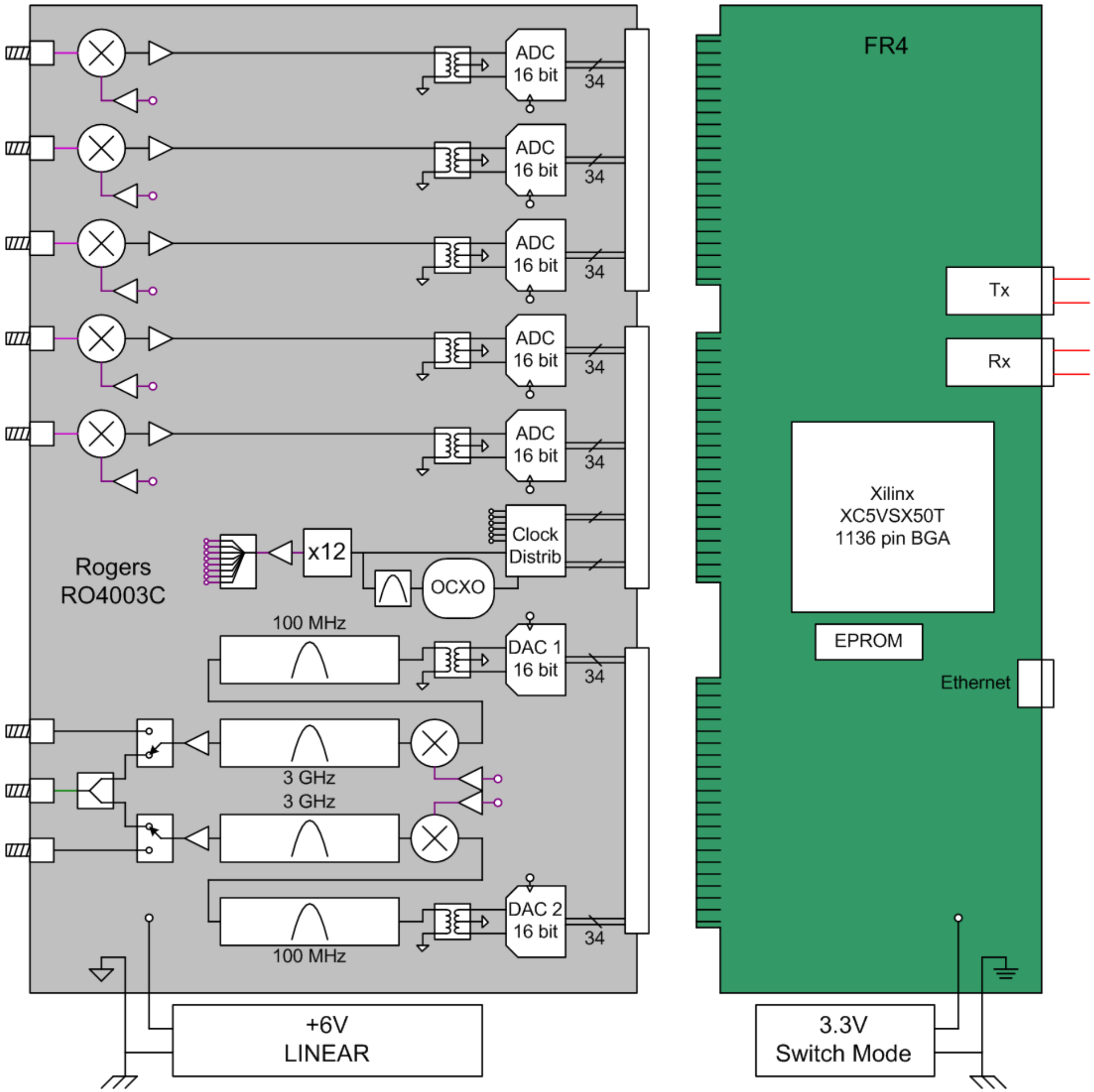


Red lines can not be actively calibrated

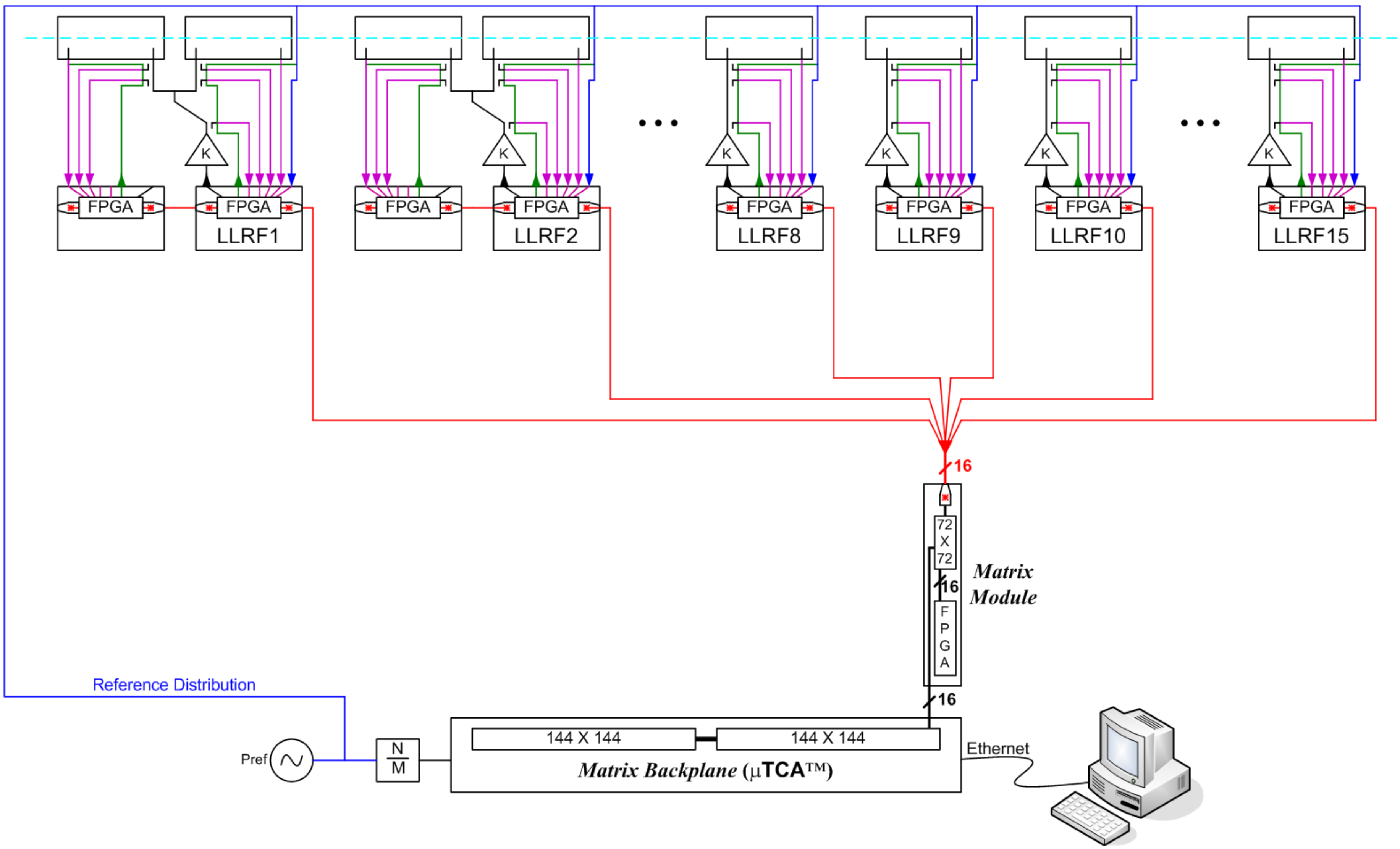
The FLLRF Control System



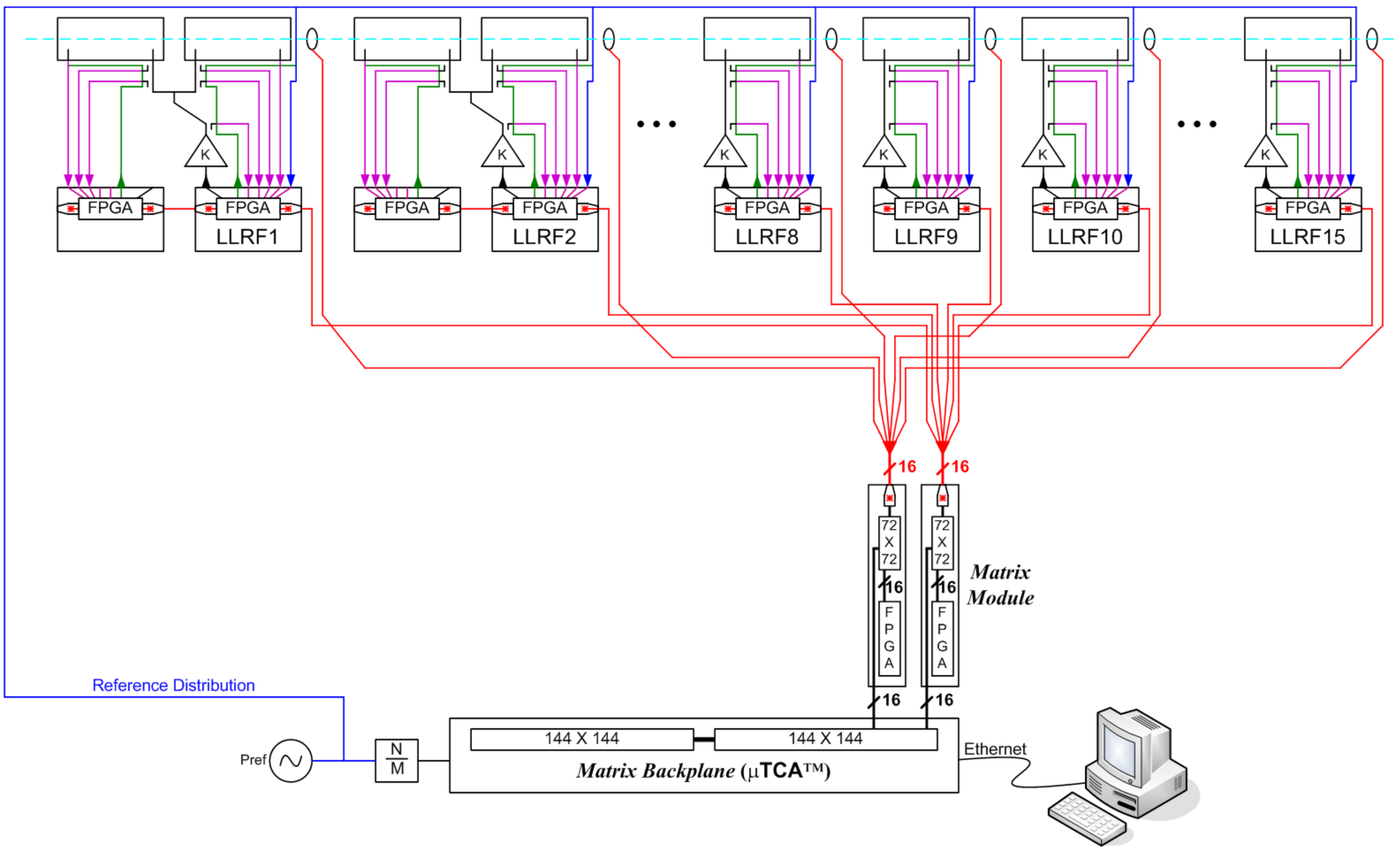
FLLRF Circuit Layout

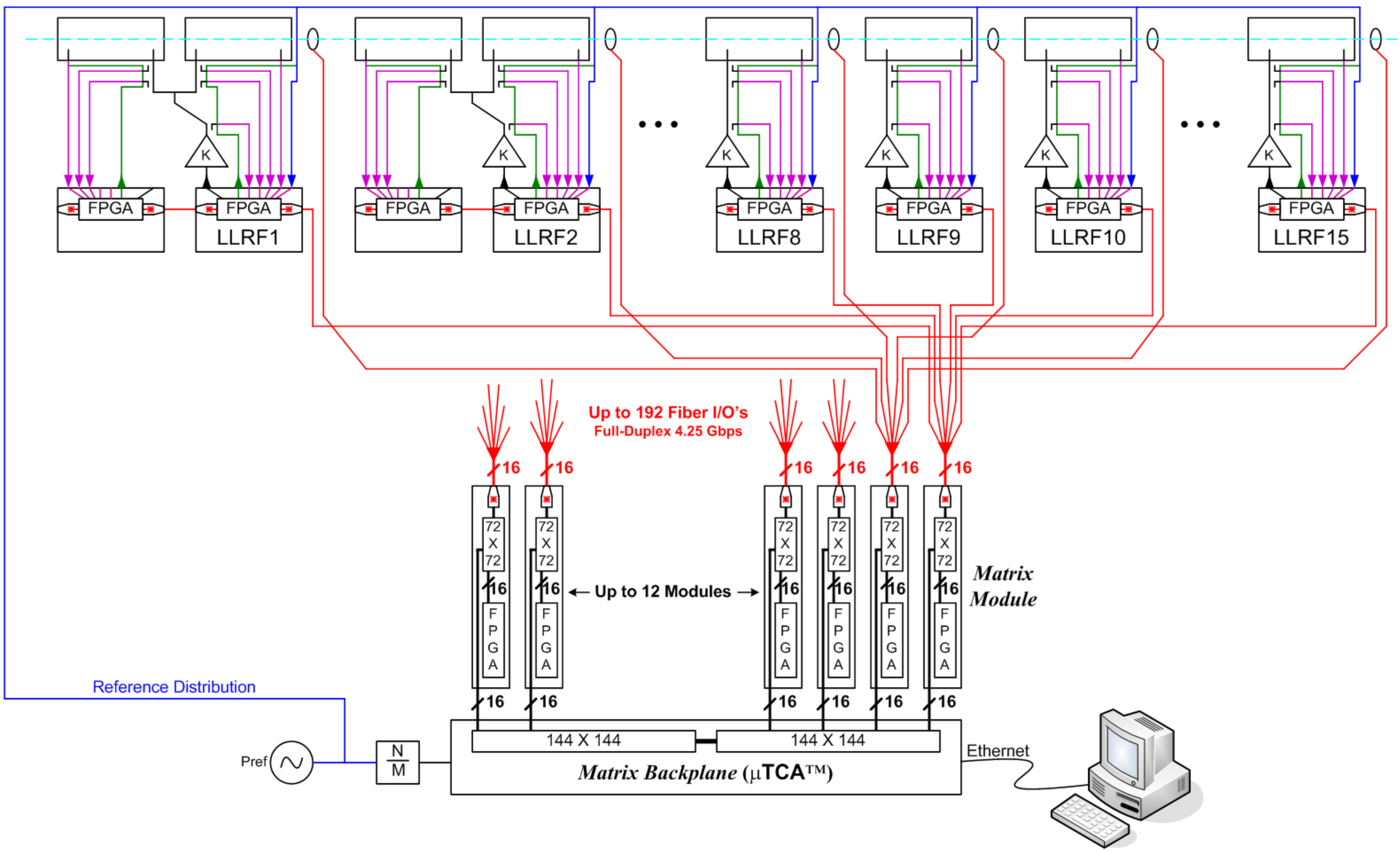


Global Communication and Control via 'The Matrix' part 1



Global Communication and Control via 'The Matrix' part 2

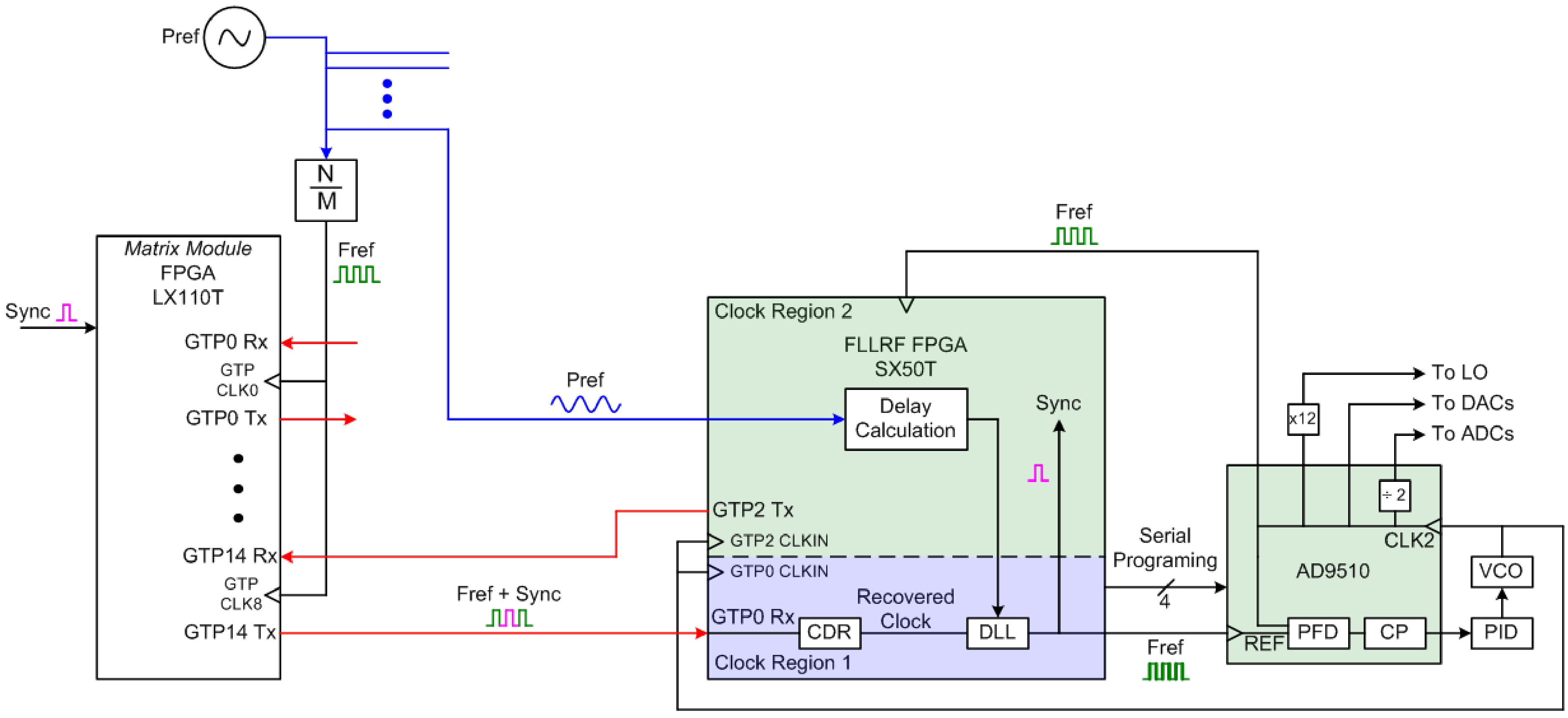




FPGA
LLRF1
LLRF2
LLRF8
LLRF9
LLRF10
LLRF15
K
Up to 192 Fiber I/O's
Full-Duplex 4.25 Gbps
16
72 X 72
F P G A
Up to 12 Modules
Matrix Module
Reference Distribution
Pref
N
M
144 X 144
144 X 144
Matrix Backplane (μTCA™)
Ethernet

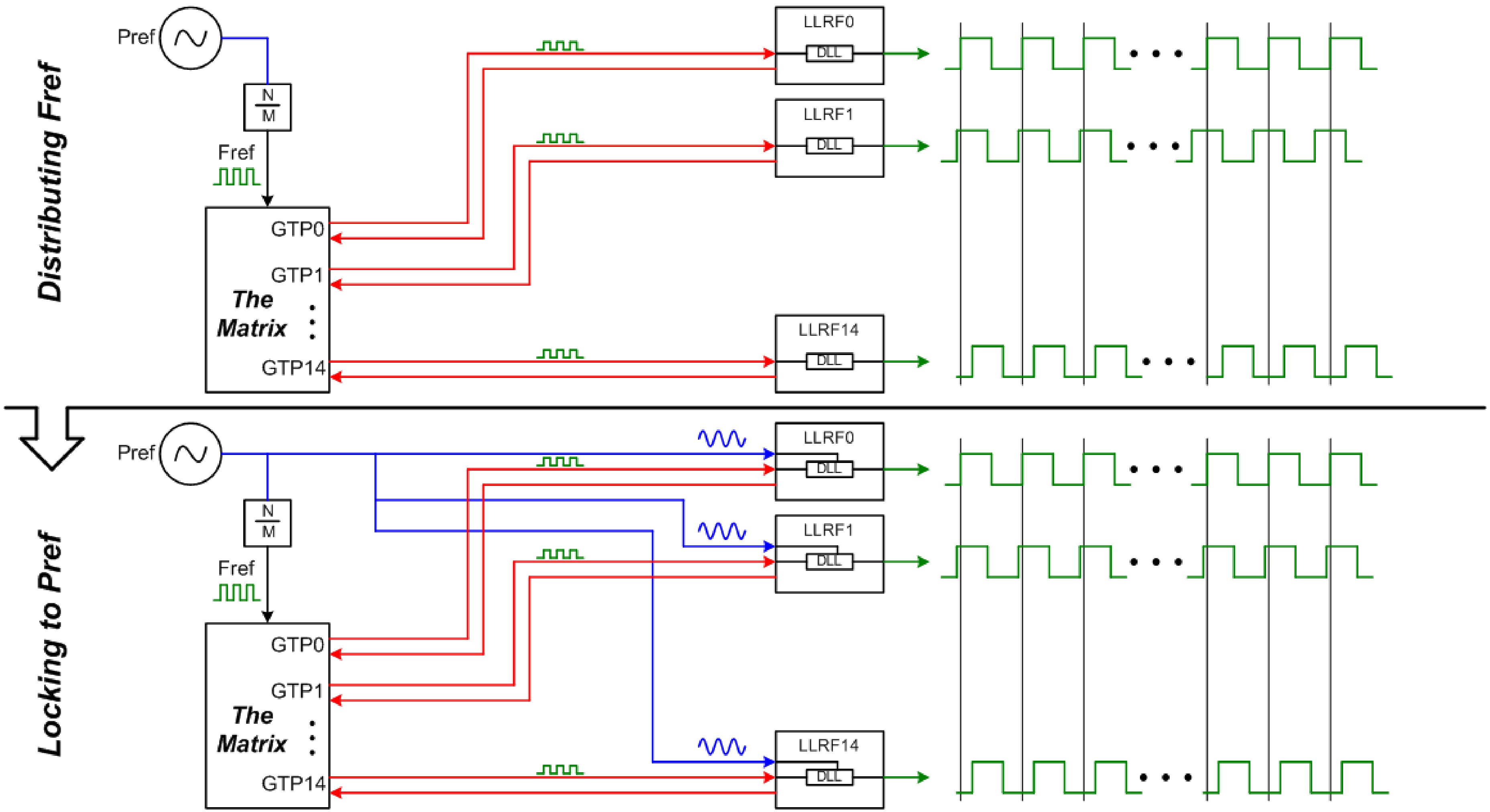
Agent Smith

Agent Stettler

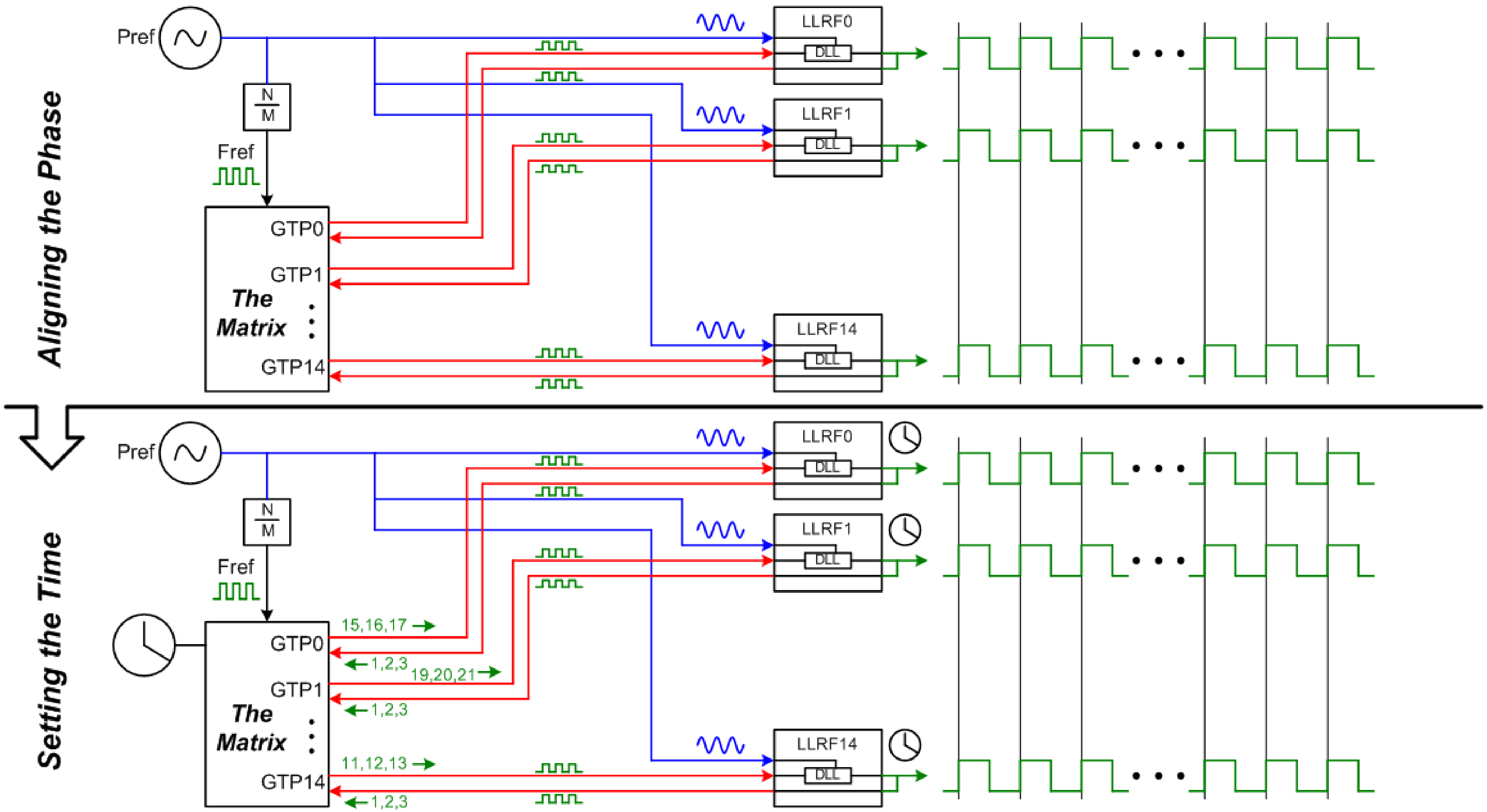


Pref
Matrix Module
FPGA
LX110T
Sync
GTP0 Rx
GTP
CLK0
GTP0 Tx
GTP14 Rx
GTP
CLK8
GTP14 Tx
N
M
Fref
Pref
Fref + Sync
Fref
Clock Region 2
FLLRF FPGA
SX50T
Delay
Calculation
Sync
GTP2 Tx
GTP2 CLKIN
GTP0 CLKIN
Recovered
Clock
GTP0 Rx
CDR
DLL
Clock Region 1
Serial
Programing
4
Fref
To LO
To DACs
To ADCs
x12
÷ 2
CLK2
AD9510
REF
PFD
CP
VCO
PID

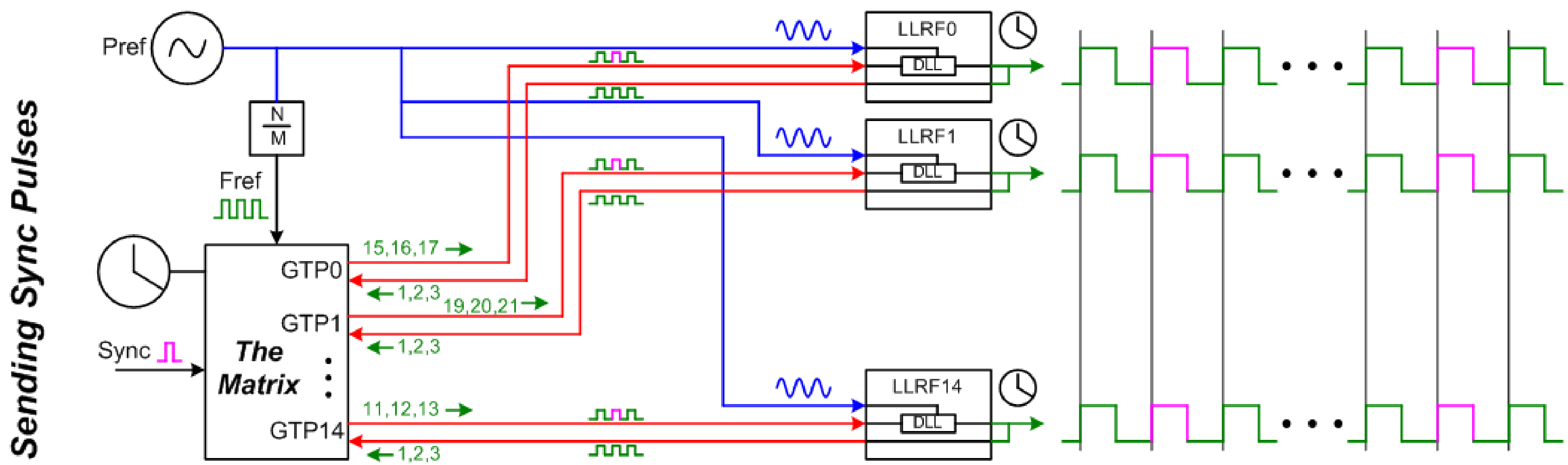
Frequency Reference, Time and Trigger Distribution Scheme



Frequency Reference, Time and Trigger Distribution Scheme



Frequency Reference, Time and Trigger Distribution Scheme



FPGA Algorithms and Code

- Algorithmic code will be done in Matlab/Simulink with Xilinx blockset or Octave (designer preference), and ported to VHDL or Verilog (designer preference).
  - Main cavity loop (Pulse-to-Pulse feedback with non-IQ sampling)
  - Klystron loop (Direct feedback with non-IQ sampling)
  - Calibration
  - Hardware error correction
  - Hardware co-simulation
- Non-algorithmic code written in either VHDL or Verilog (designer preference).
  - Timing and clock distribution
  - Diagnostics and history
  - Communication to The Matrix or adjacent system via GTP
  - Communication to local Ethernet
  - Other wrapping code

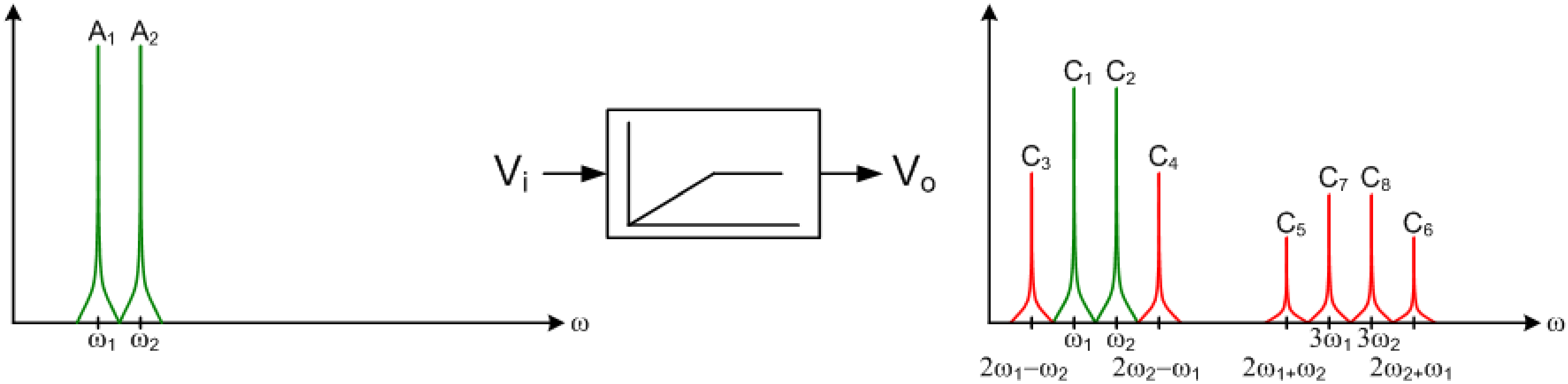
Manpower: 16 Engineers at 3 labs (ST, LBNL, CERN)

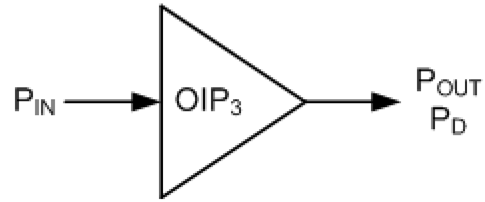
Schedule: Proof of principle prototype in 12 months

Full prototype in 18 to 24 months

The Fermi team at Sincrotrone Trieste

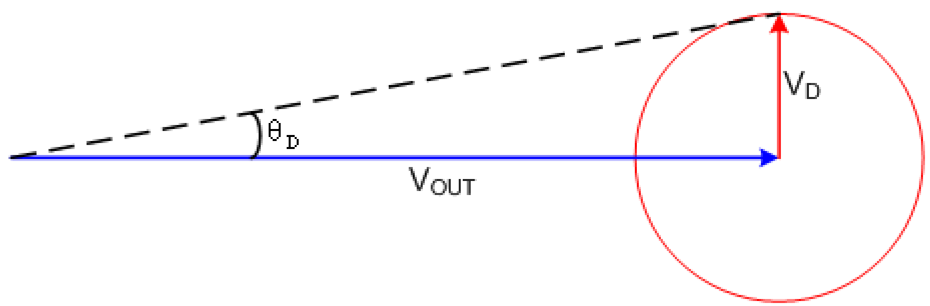
Saturation: A cause of distortion (IP3)





P_{IN} = Input Signal Power (dBm)
P_{OUT} = Output Signal Power (dBm)
P_D = 3rd Order Distortion Power (dBm)
OIP_3 = Device Output IP_3 (dBm)

$$P_D = 3\,P_{OUT} - 2\,OIP_3$$

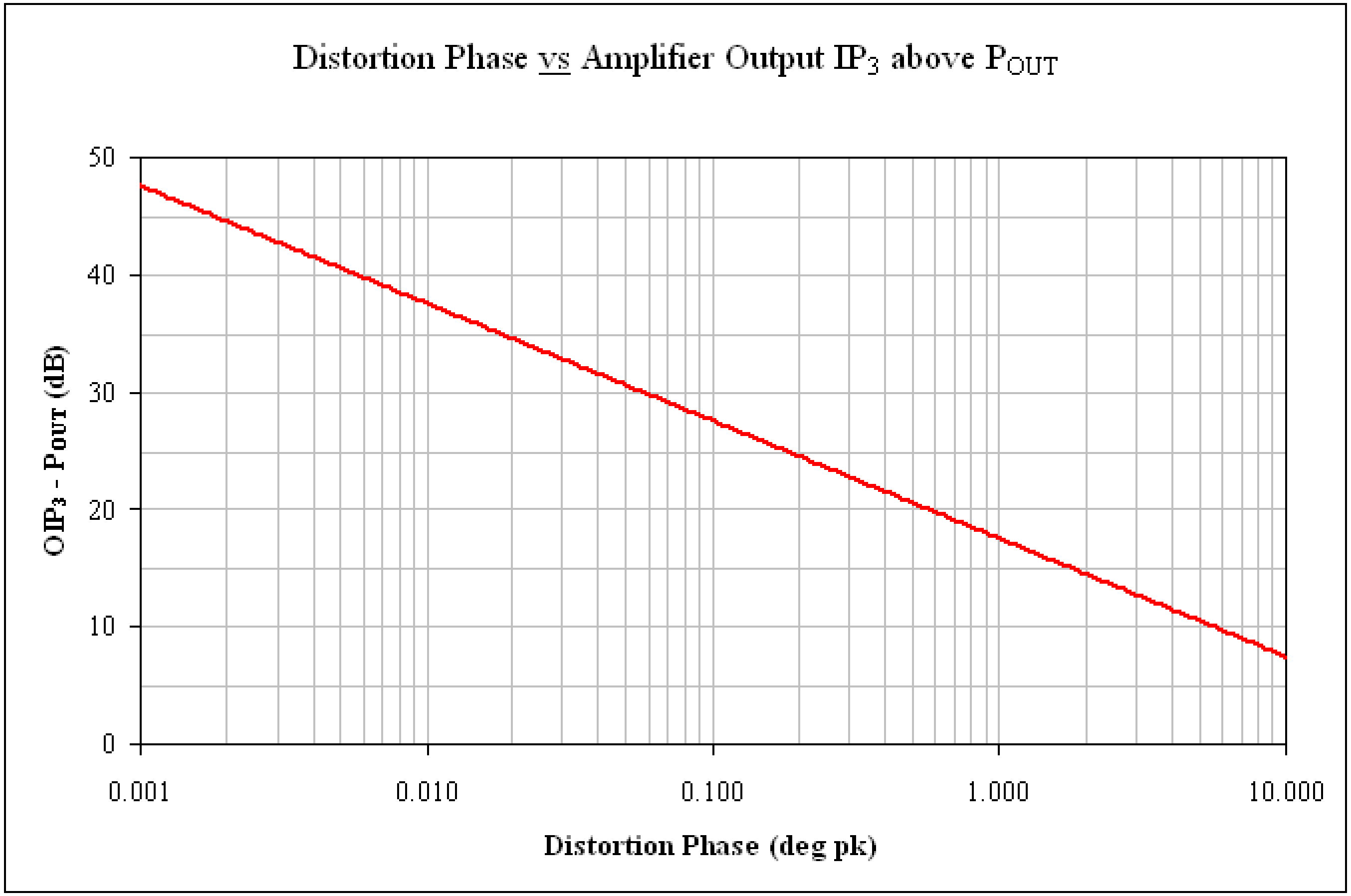


θ_{Dpk} = Distortion Phase (radians pk)
V_{OUT} = Output Signal Voltage (V pk)
V_D = Distortion Voltage (V pk)

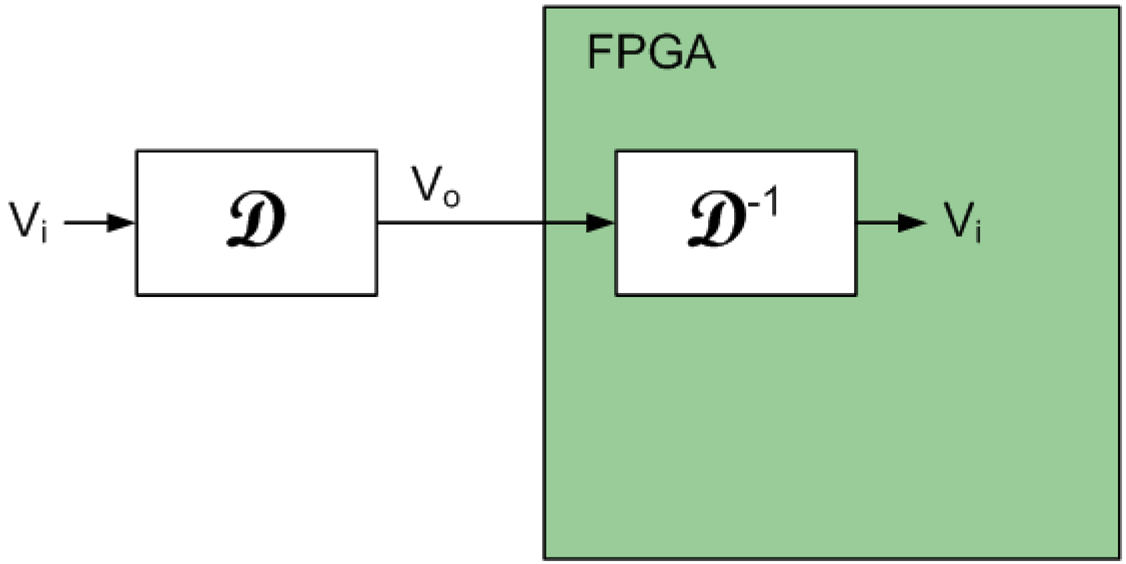
$$\theta_{Dpk} = \tan^{-1}\left(\frac{V_D}{V_{OUT}}\right)$$

Saturation (IP3) and its effects on phase accuracy

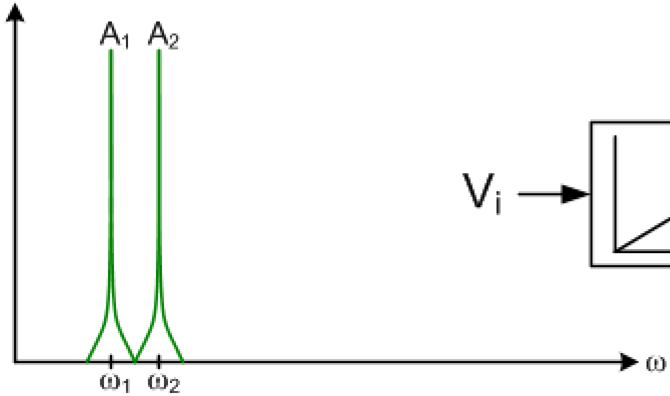
$$OIP_3 = P_{OUT} - 10\,\mathrm{Log}(\tan\theta_{Dpk})$$

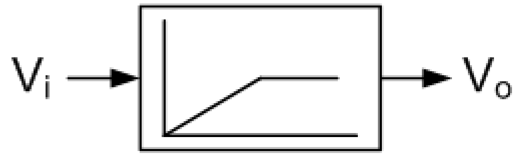


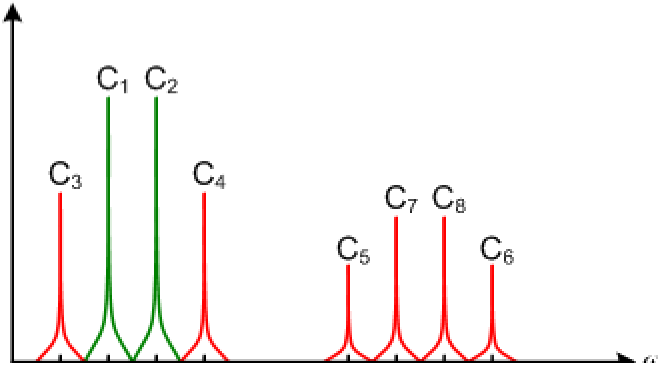
Correcting for Saturation (IP3) Strategy: Model and Invert

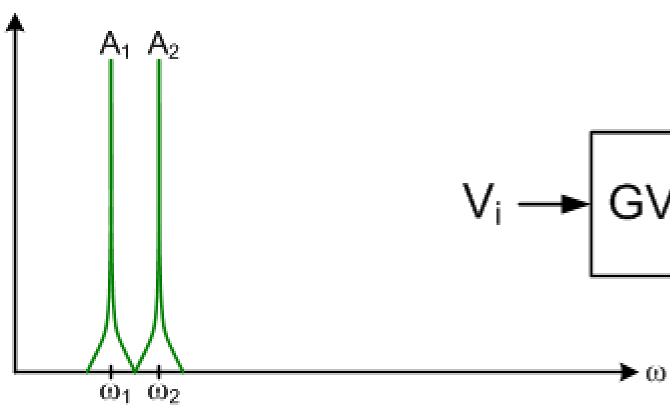


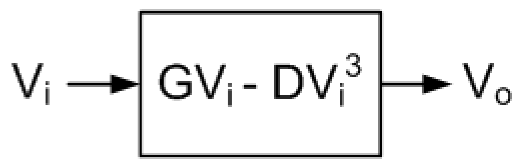
Correcting for Saturation (IP3): Model

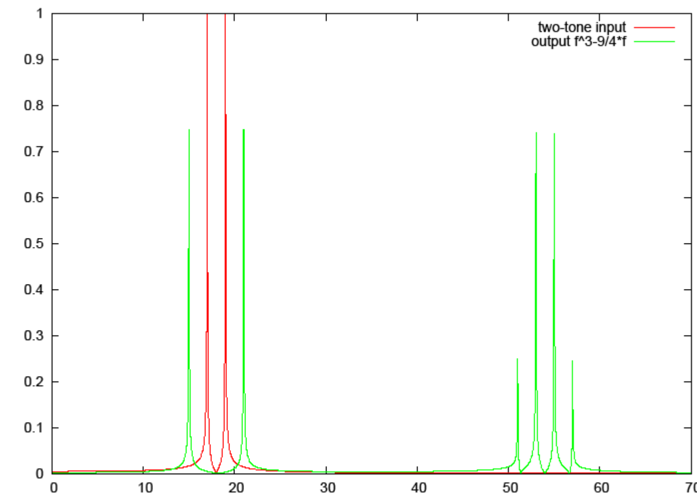


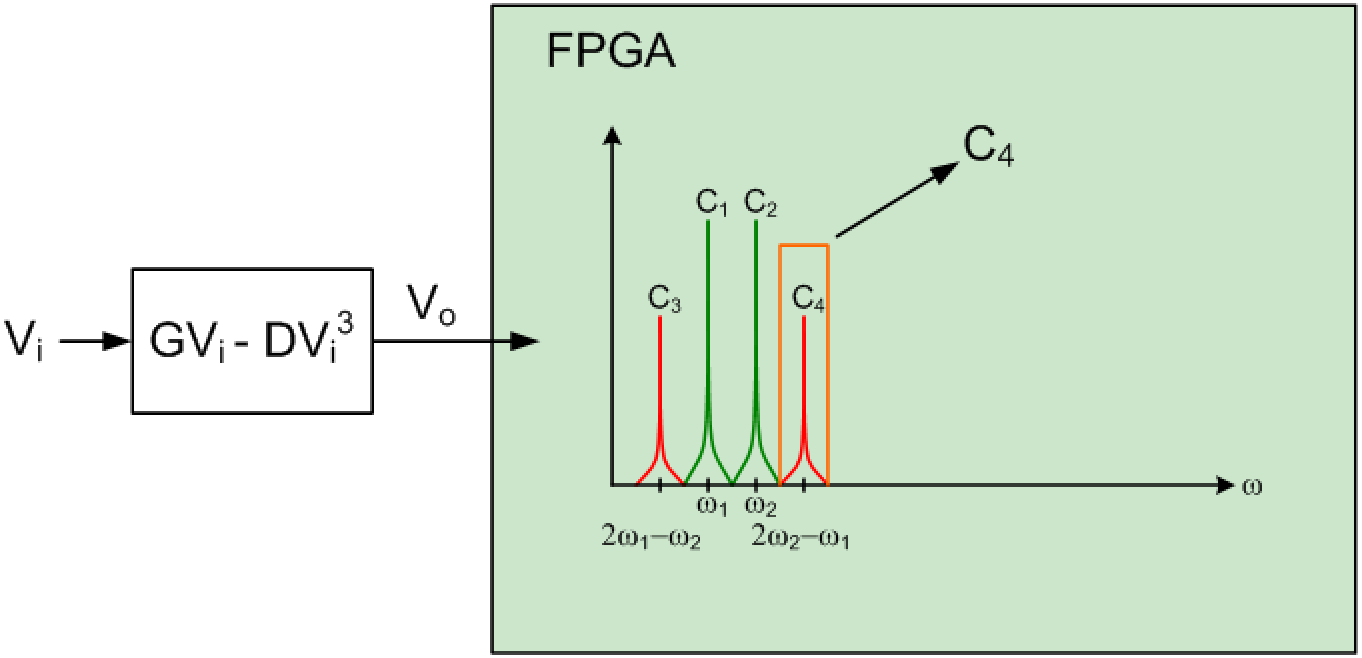












$$C_1 = GA_1 - \frac{3}{4}DA_1^3 - \frac{3}{2}DA_1A_2^2$$
$$C_2 = GA_2 - \frac{3}{4}DA_2^3 - \frac{3}{2}DA_1^2A_2$$
$$C_3 = -\frac{3}{4}DA_1^2A_2$$
$$C_4 = -\frac{3}{4}DA_1A_2^2$$

$$D = -\frac{4C_3}{3A_1^2A_2} = -\frac{4C_4}{3A_1A_2^2}$$

$$G = \frac{C_1}{A_1} - \frac{C_4}{A_1}\left(\frac{A_1^2}{A_2^2} + 2\right) = \frac{C_2}{A_2} - \frac{C_3}{A_2}\left(\frac{A_2^2}{A_1^2} + 2\right)$$

Correcting for Saturation (IP3): Extracting the original V_i

Direct?

$$V_i(V_o) = \frac{1}{\sqrt[3]{D}}\left(\sqrt[3]{-\frac{V_o}{2}+\sqrt{\frac{V_o^2}{4}-\frac{G^3}{27D}}}+\sqrt[3]{-\frac{V_o}{2}-\sqrt{\frac{V_o^2}{4}-\frac{G^3}{27D}}}\right)$$

NO.

Taylor Expansion?

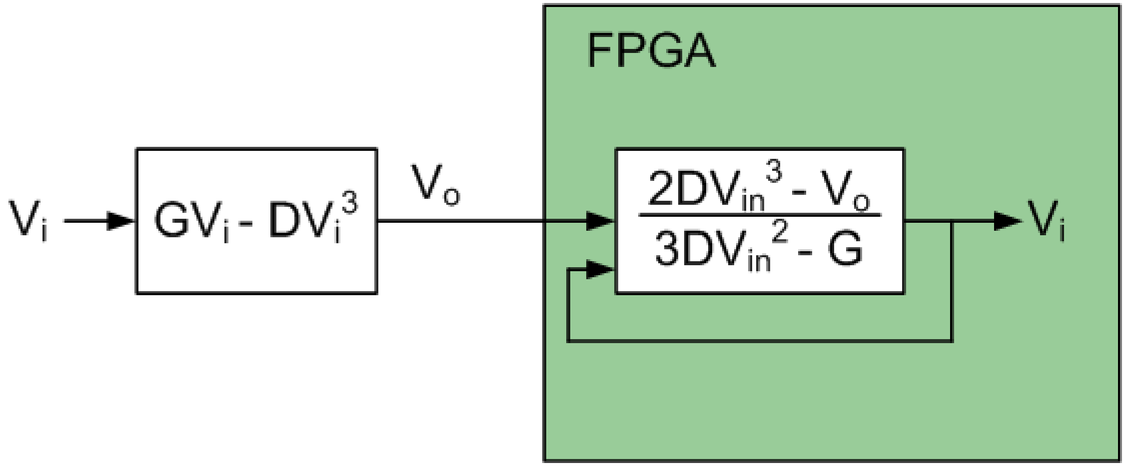
$$V_i(x) = \sum_{n=0}^{\infty}\frac{1}{n!}\frac{d^n V_i(c)}{dV_o^n}(x-c)^n$$

PLEASE NO!

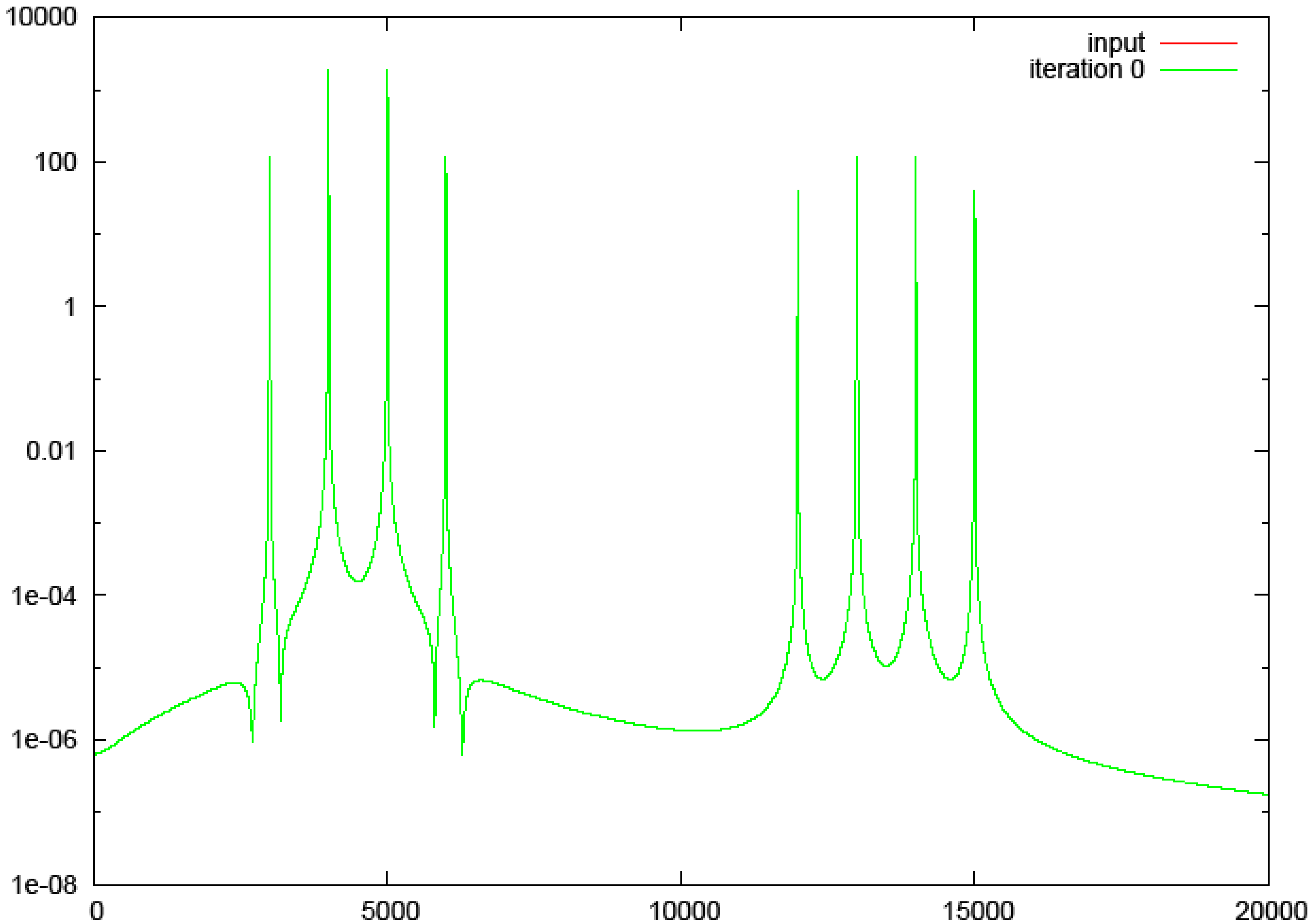
Newton's Method?

$$V_{i_{n+1}} = V_{i_n} - \frac{f(V_{i_n})}{f'(V_{i_n})} = \frac{2DV_{i_n}^3 - V_o}{3DV_{i_n}^2 - G}$$

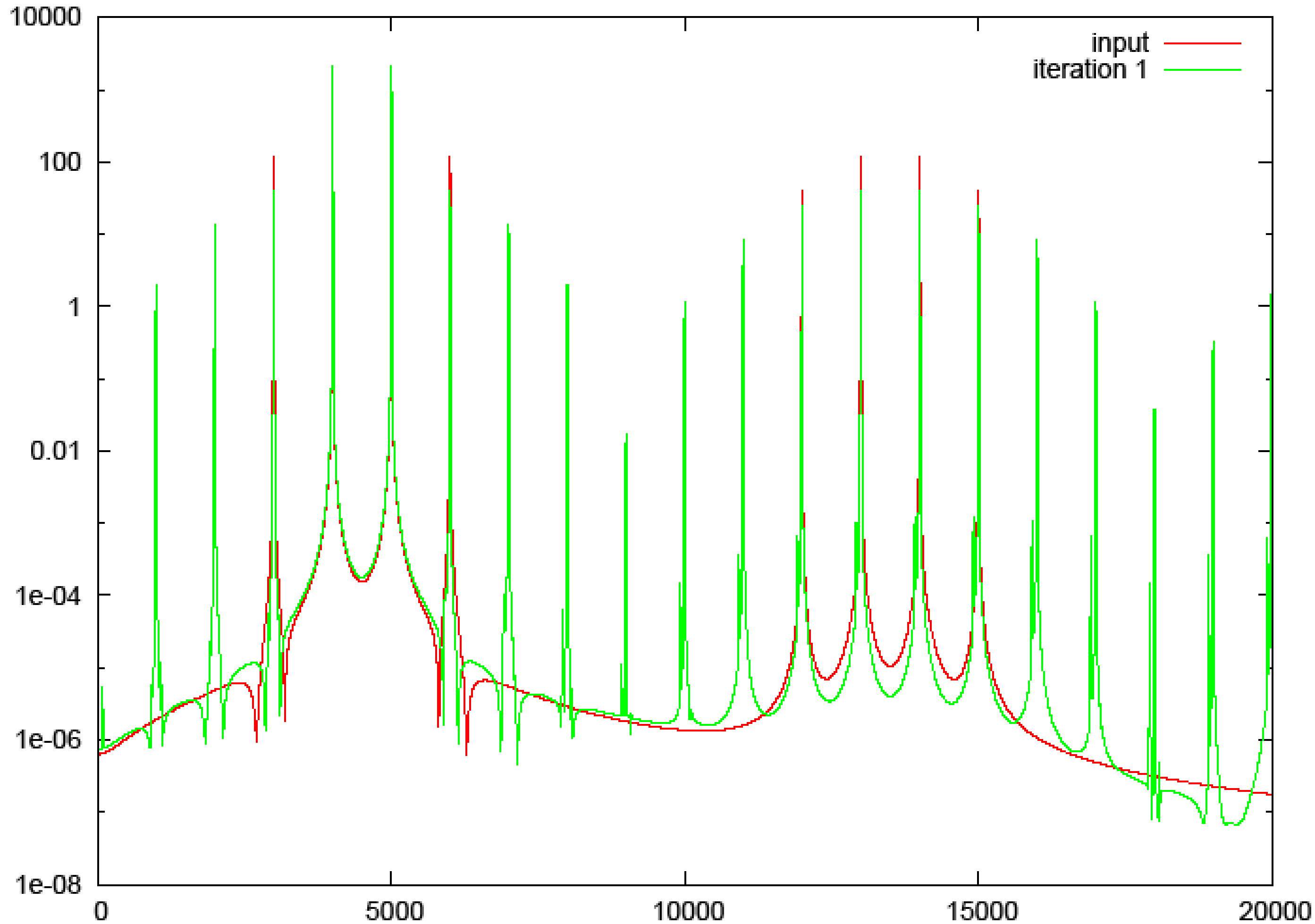
Newton's Method in an FPGA



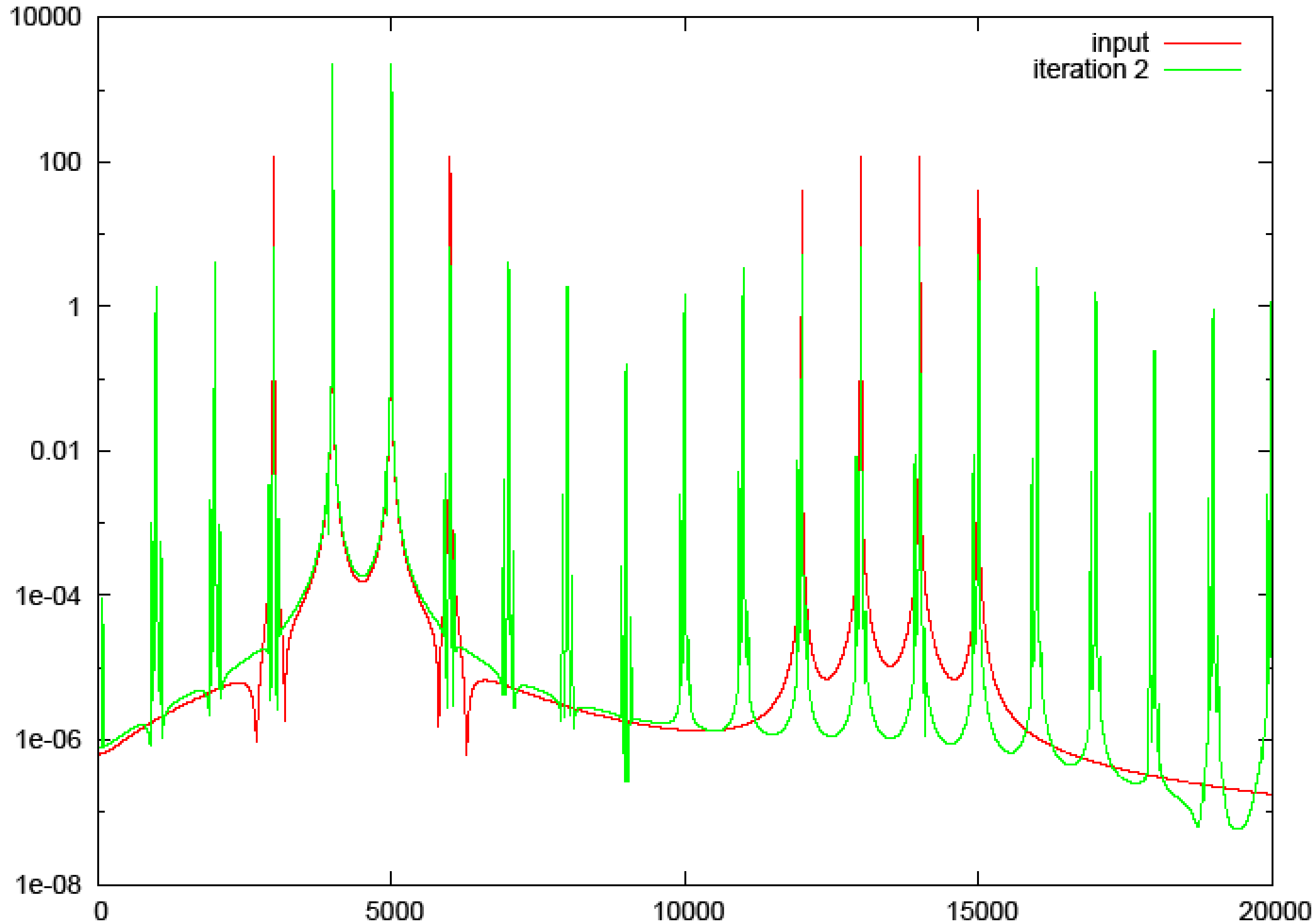
Correcting for Saturation (IP3): Extracting the original V_i



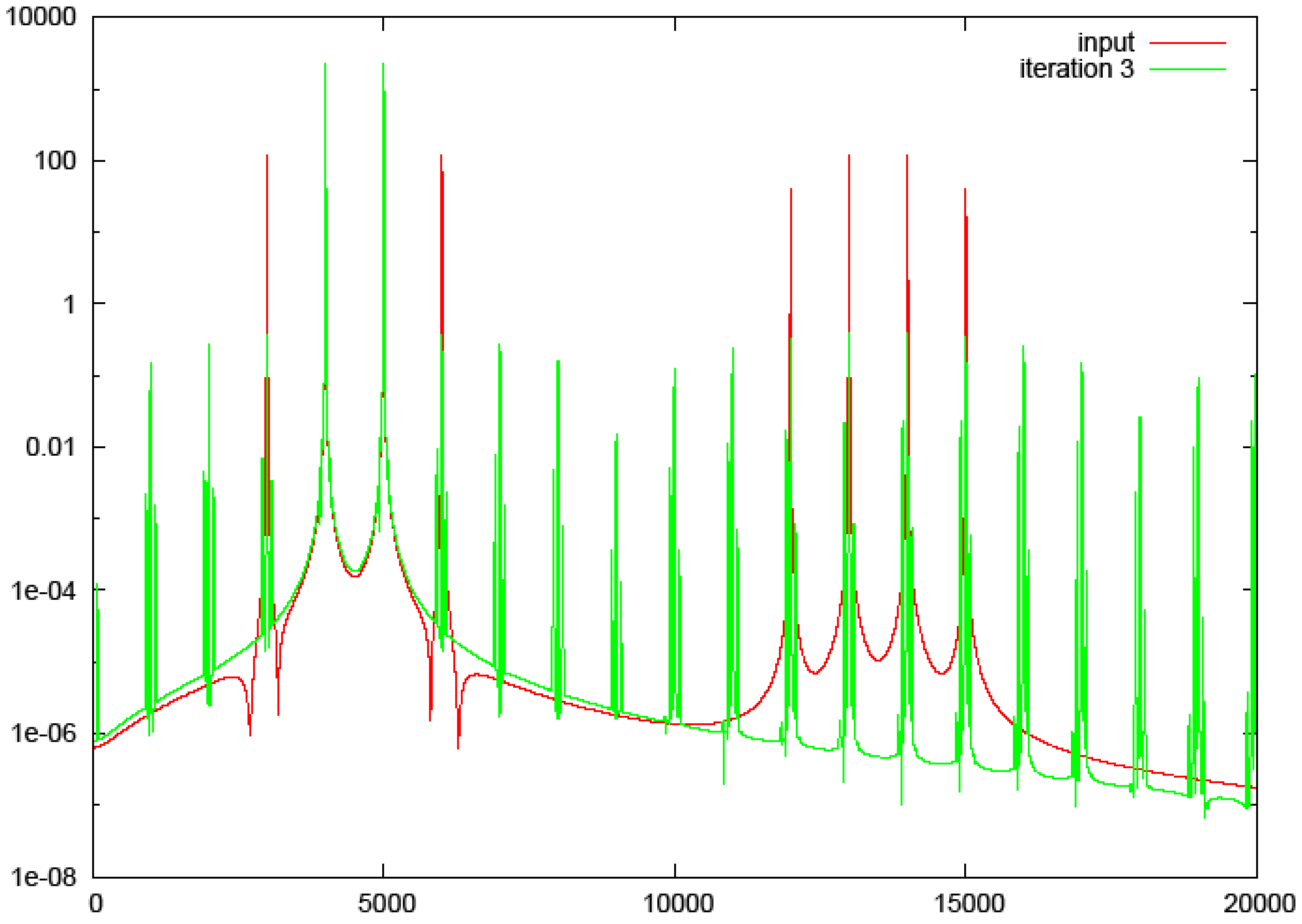
Correcting for Saturation (IP3): Extracting the original V_i



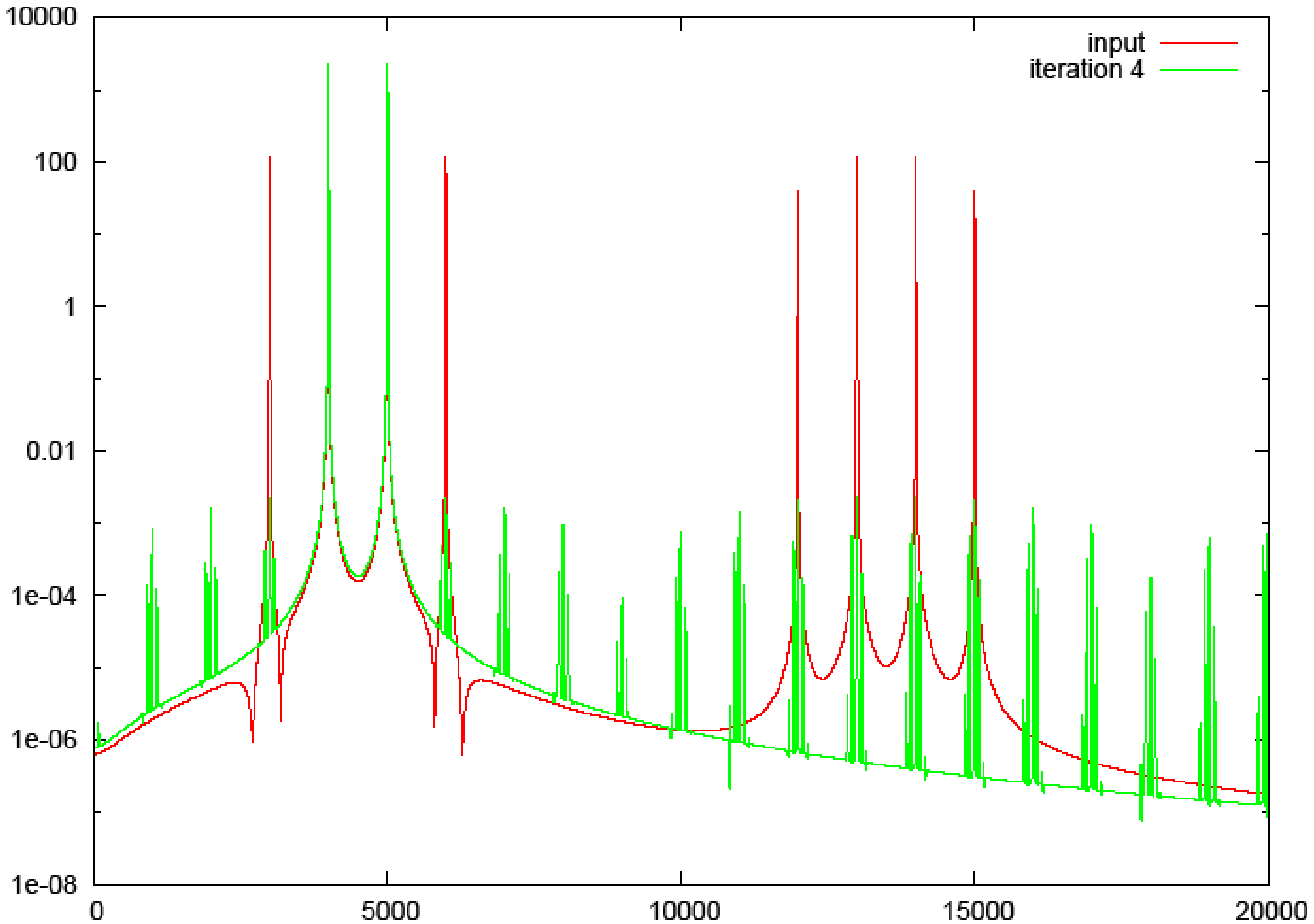
Correcting for Saturation (IP3): Extracting the original V_i



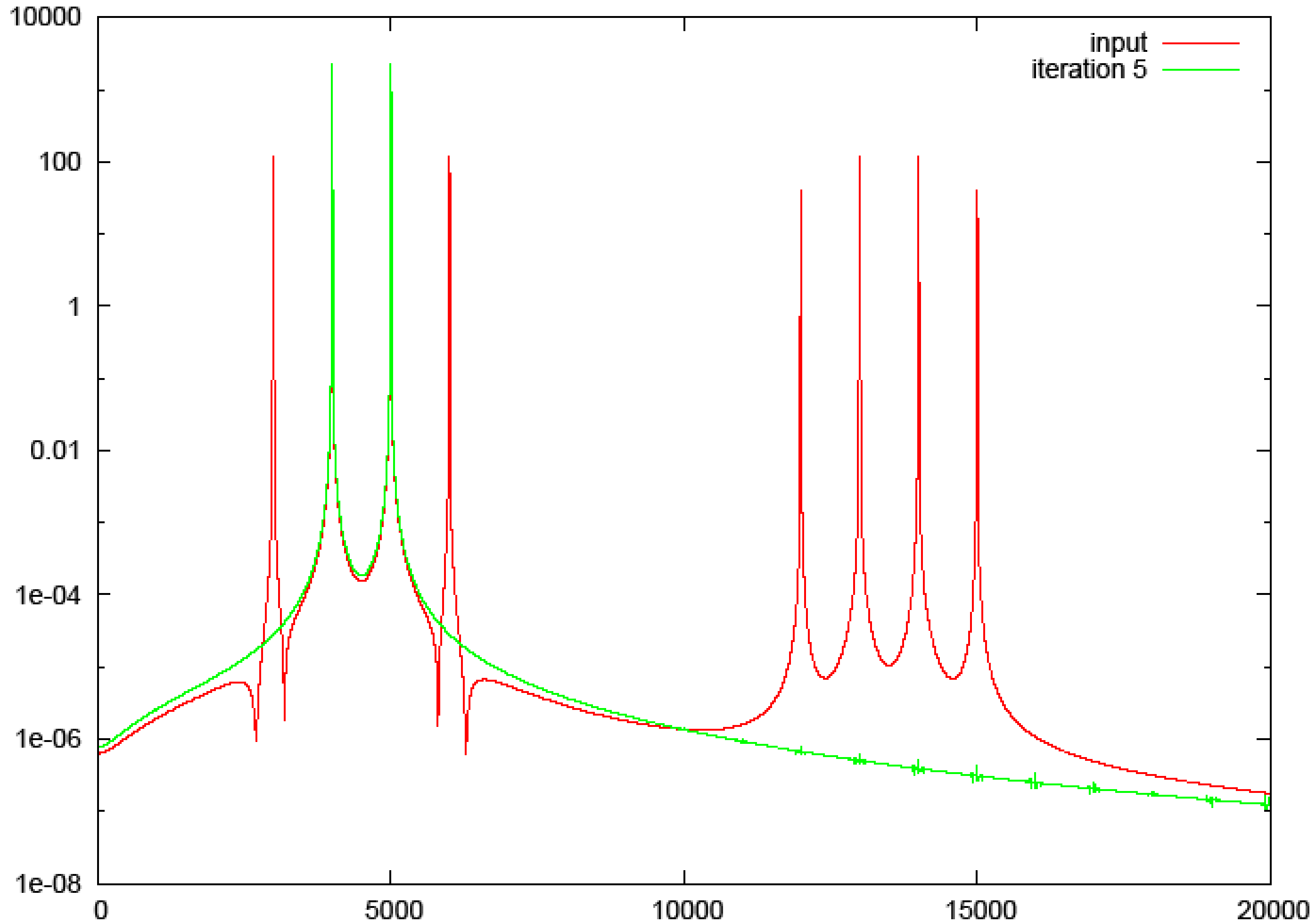
Correcting for Saturation (IP3): Extracting the original V_i



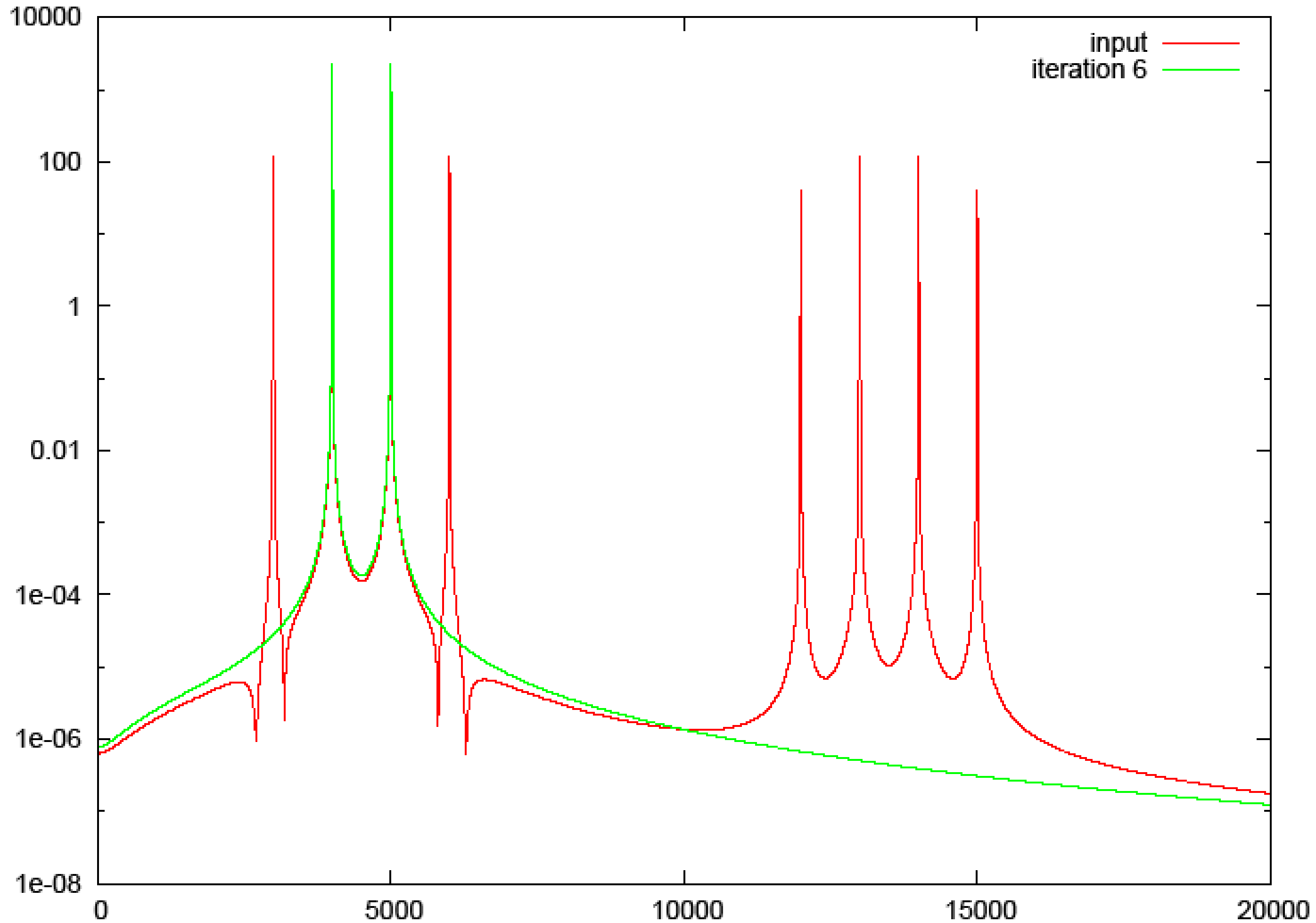
Correcting for Saturation (IP3): Extracting the original V_i



Correcting for Saturation (IP3): Extracting the original V_i



Correcting for Saturation (IP3): Extracting the original V_i



Conclusion: Live a better life through FPGA's!