

Digital LLRF for ALBA Storage Ring

-RF & Diagnostics Section -

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ALBA Overview

ALBA Schedule

Storage Ring RF Plants

Digital LLRF Conceptual Design: Controls and Diagnostics

DLLRF Hardware

- Digital boards: Sundance and Lyrtech

- Analog Front Ends

- Timing Systems

- Control Loops: Amplitude, phase and tuning

Diagnostics

Test Results

- ALBA is a 3rd generation synchrotron light source, located at 20 km from Barcelona, Spain.



Picture August 07

➤ Main parameters

Energy	3 GeV
Circumference	268m
Beam current	400mA
Emittance	4 nm.rad
Lifetime	≈10h
RF Freq	500MHz
Beamlines	7 at day 1

➤ Linac

Installation and commissioning

January – April 2008

➤ Booster

Installation starts

April 2008

Pre – Commissioning

November 2008

➤ Storage Ring

Installation

June – December 2008

Sub-components commissioning

January - March 2009

Commissioning starts

April 2009

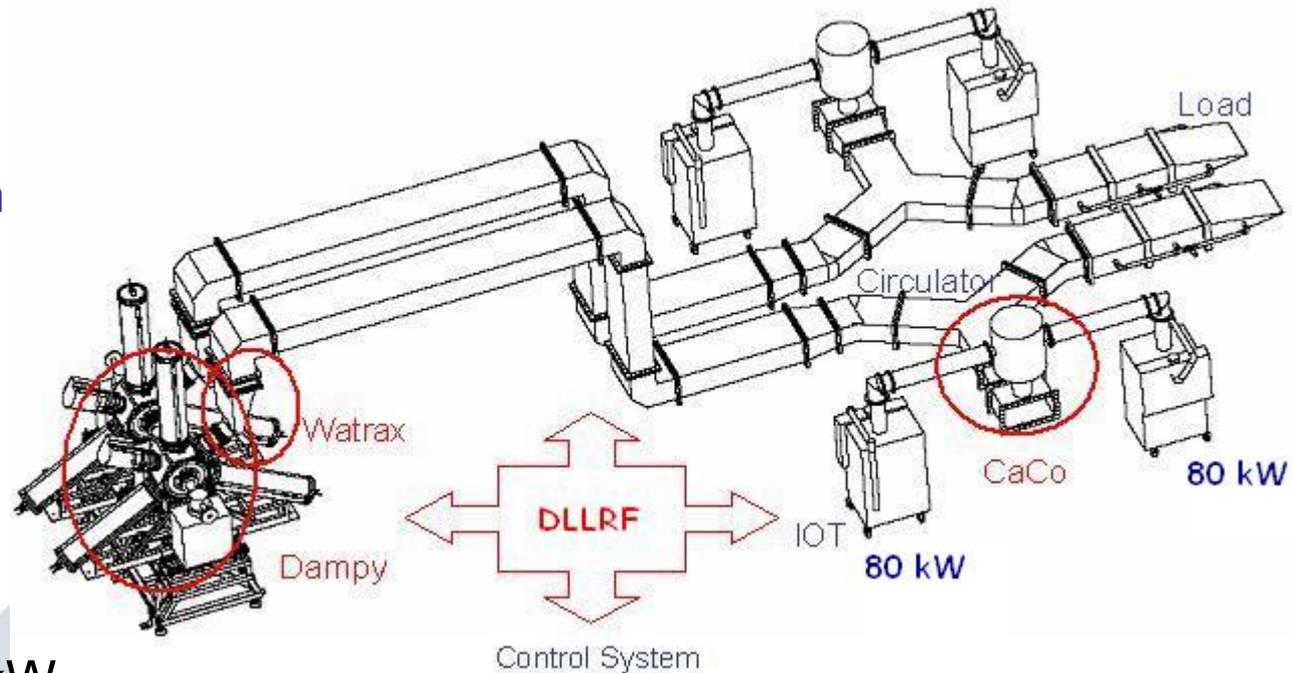
First Beam to Beamlines

June 2009

Open for users

May 2010

RF Parameters

 U_0 1.3MeV/turn V_{total} 3.6 MV q ≈ 2.5 f_s ≈ 9 kHz P_{RF} 960kW

6 RF Plants of 160kW

2 IOT Transmitters per RF cavity. Power combined in CaCo

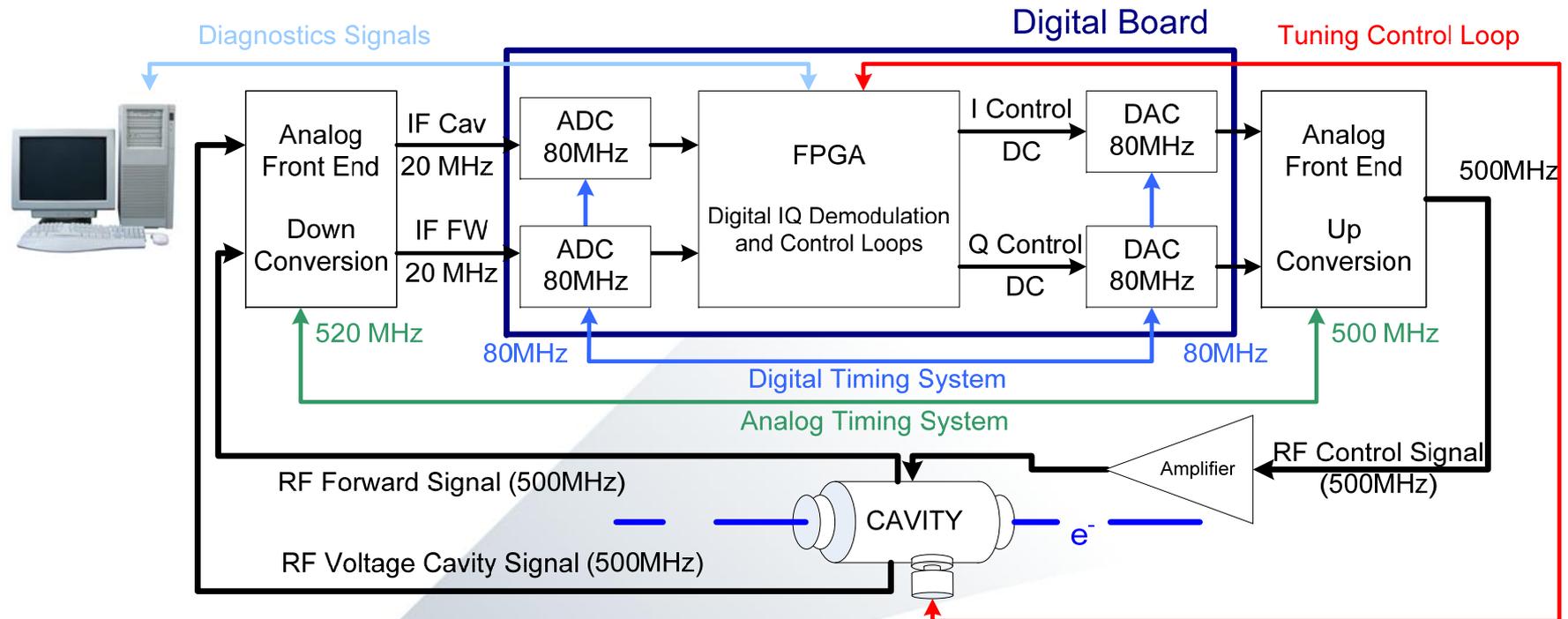
Dampy Cavity

Normal Conducting

Single cell, HOM damped

3.3 M Ω

Digital LLRF System based on IQ mod/demod



Conceptual Design and Prototype

Digital Commercial Board: cPCI with 2 ADCs, 2 DACs and FPGA

Analog Front Ends for Downconversion (RF to IF) and Upconversion (DC to RF)

Timing systems: 520MHz for downconversion synchronized with digital 80MHz clock for digital acquisition

RF Signals: IQ digital demodulated

➤ Cavity

Cavity Power

Forward and Reversed Cavity Power

➤ Waveguide System

Fw and Rv Circulator Input

Fw and Rv Circulator Output

Fw and RV Load Power

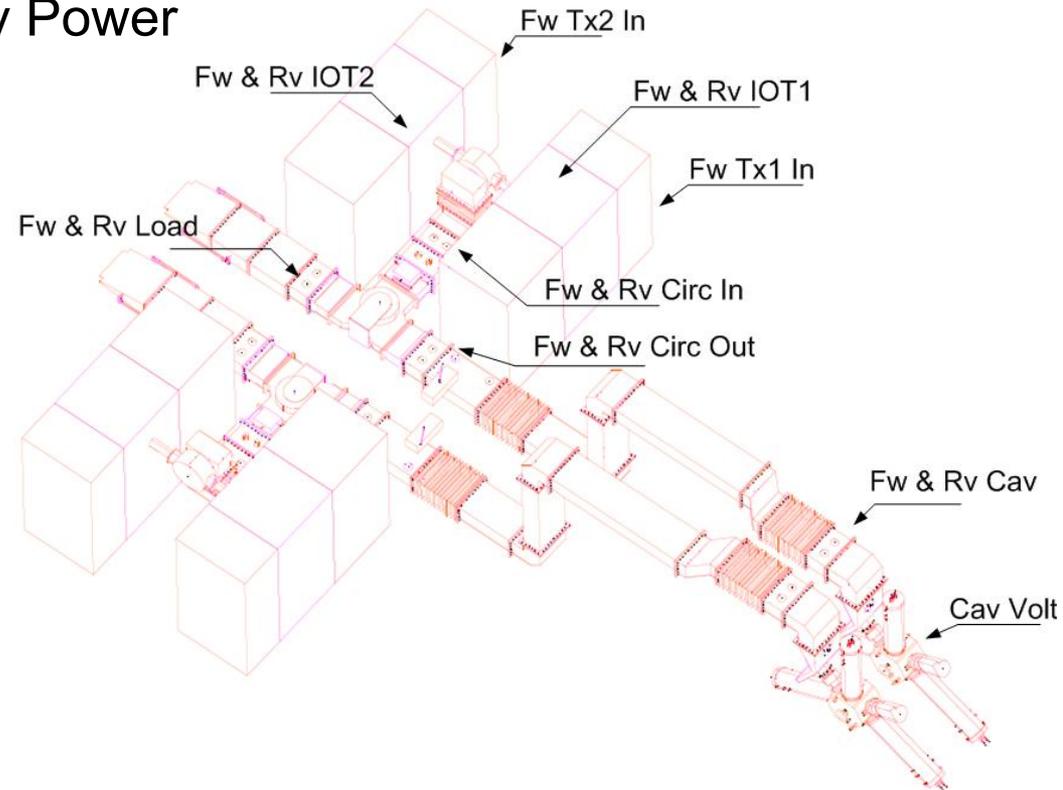
➤ Transmitter Signals

Fw Transmitter1 Input Power

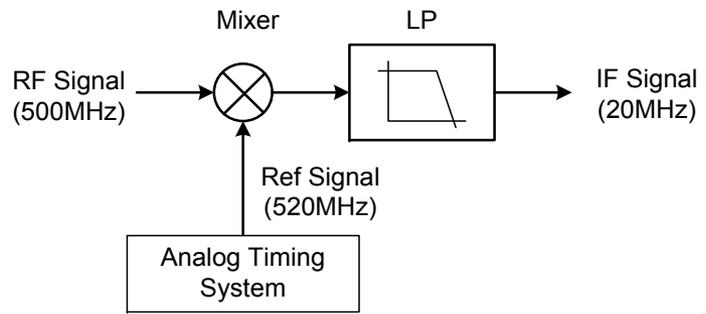
Fw Transmitter2 Input Power

Fw and Rv IOT-01 Power

Fw and Rv IOT-02 Power

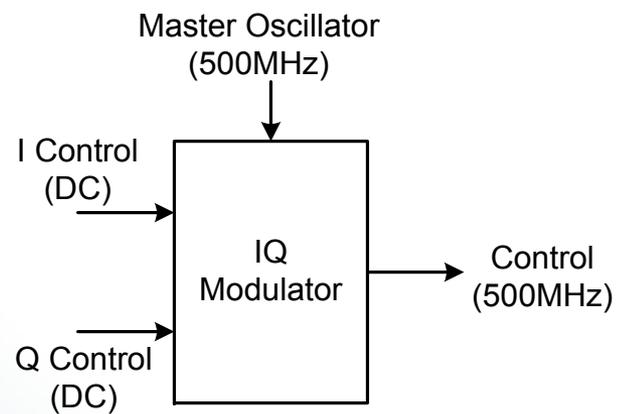


➤ Downconversion: From RF to IF

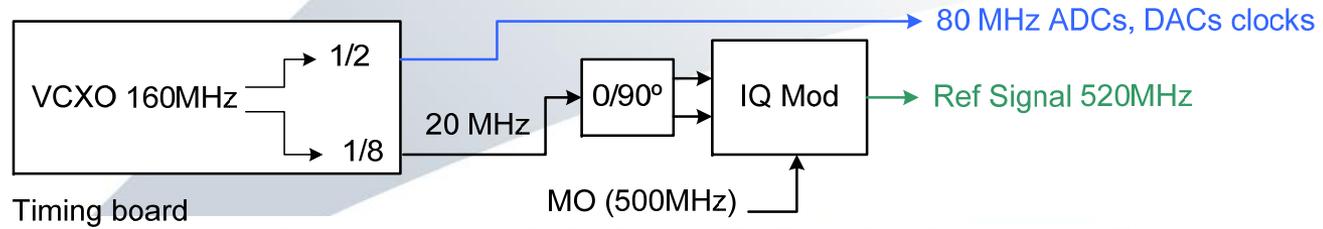


Ref Signal (520MHz) = MO + IF
ADCs Clock = 4*IF

➤ Upconversion: From DC to RF



➤ Timing System



Front End and timing system crate

➤ Sundance: Software Defined Radio kit



Carrier Board: PCI format

DSP Daughter board: 600MHz 64 bit DSP

FPGA Daughter board for control loops:

2 ADCs 105 MHz, 14 bits

2 DACs 140MHz, 16 bits

FPGA: Virtex II

2 FPGA Daughter board for RF diagnostics:

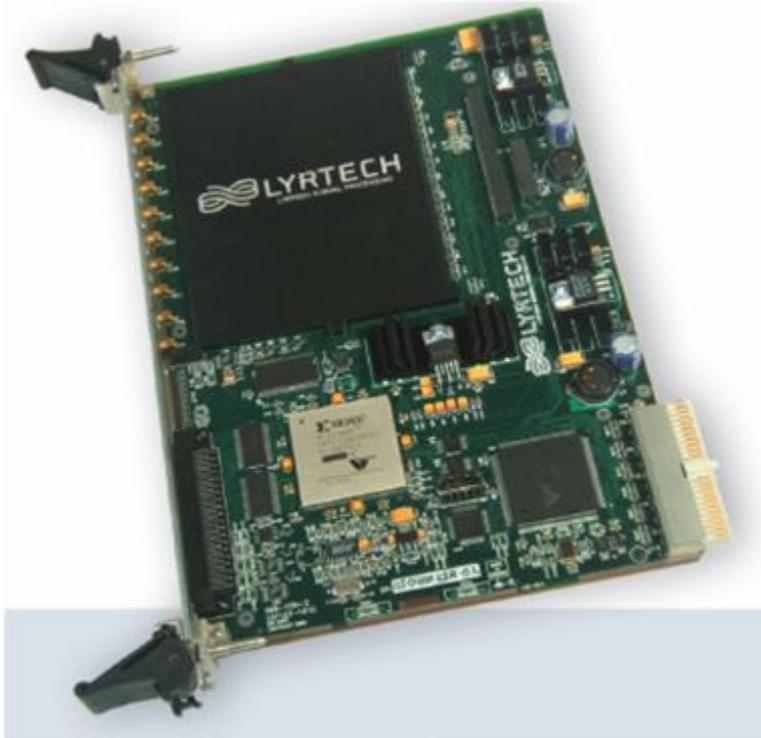
8 ADCs 10MHz (IQ Demod + undersampling)

FPGA: Virtex

Control Loops: Tested and working

Diagnostics boards:
Encountered some communications problems

➤ Lyrtech: VHS ADAC-4



cPCI format

2 x 8 ADCs 125 MHz 14 bits

8 DACs 125MHz 14 bits

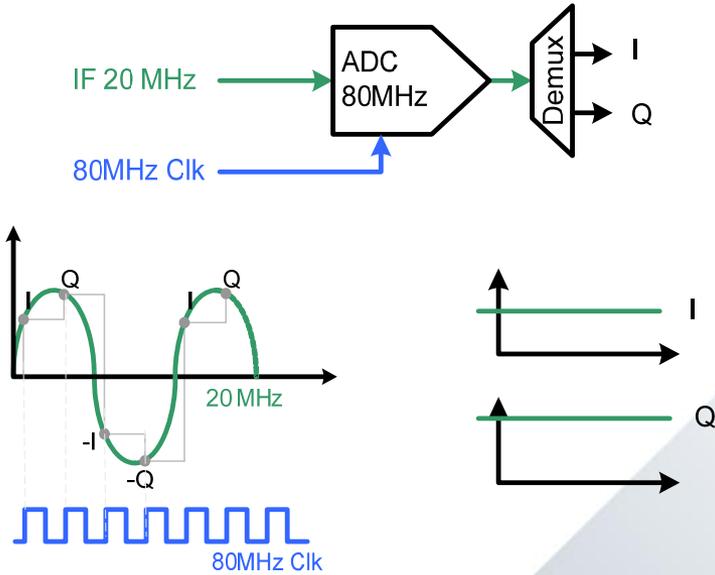
Virtex 4

128 Mbytes RAM

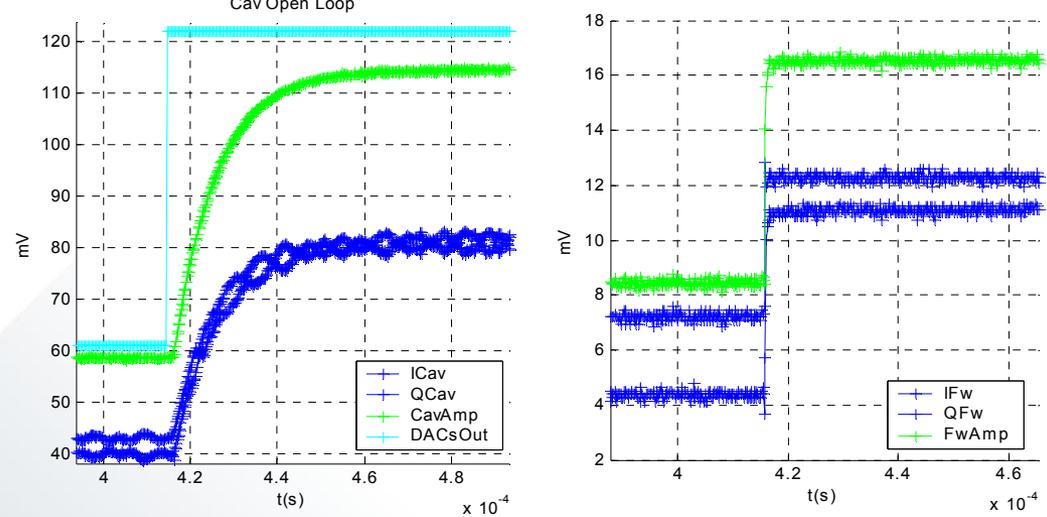
Migration from Sundance hardware to
Lyrtech hardware one week/man

Control Loops and Diagnostics: Tested and
working

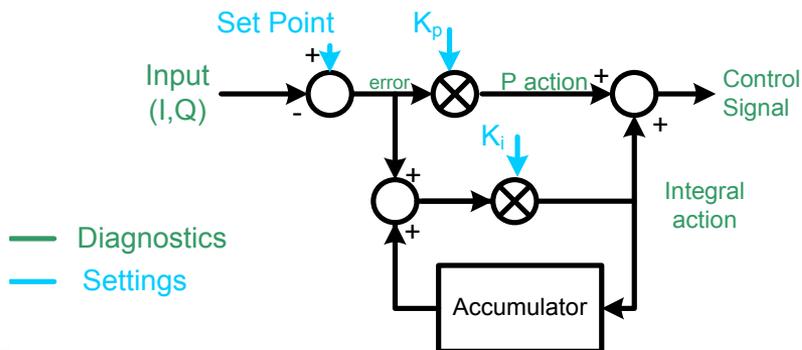
Digital IQ Demodulation



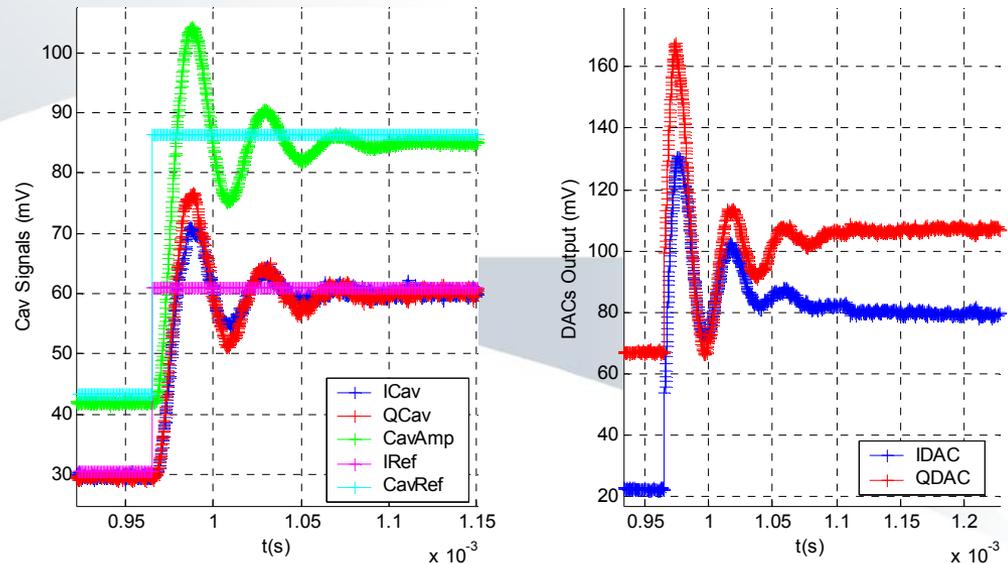
Step response in Open loop (Cav&Fw)



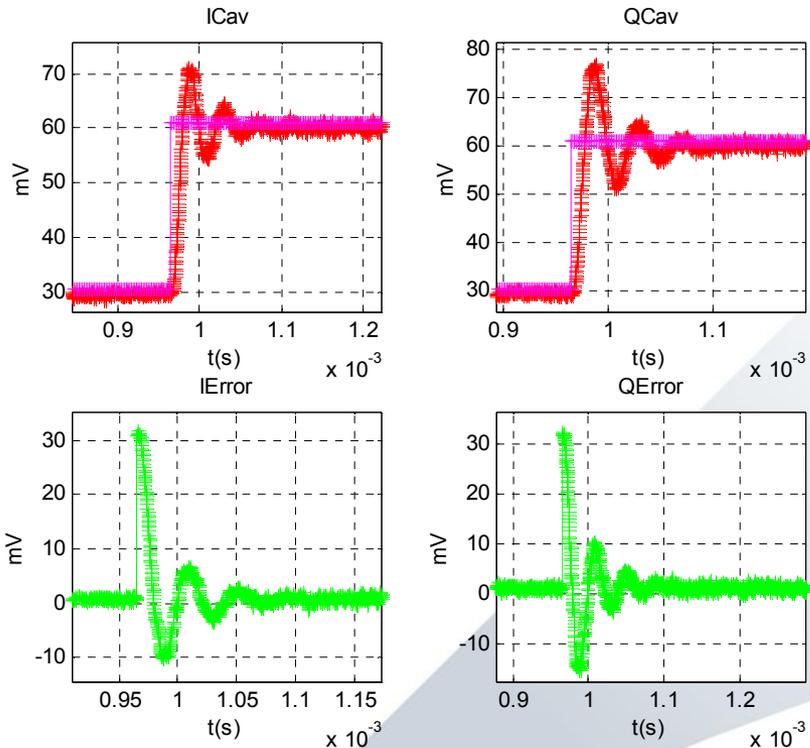
PID Control Loop for IQ



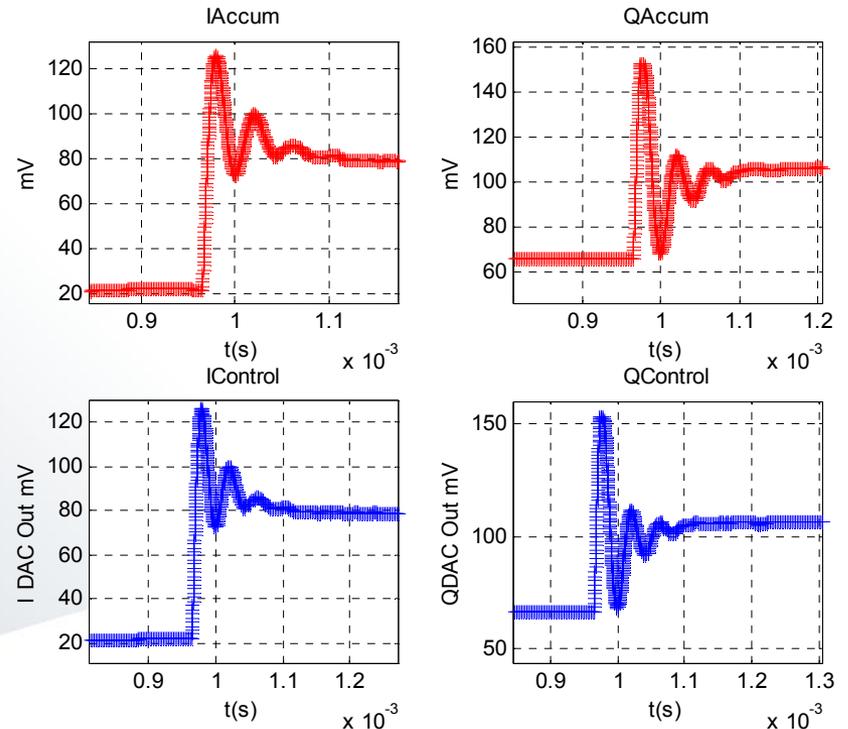
Step response in Close Loop (Cav&DACs)



I&Q Cav Signals and errors



PID Component and Outputs



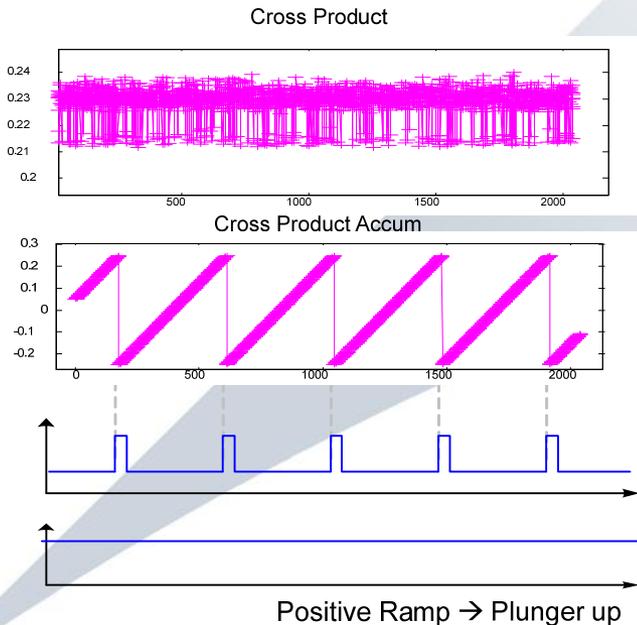
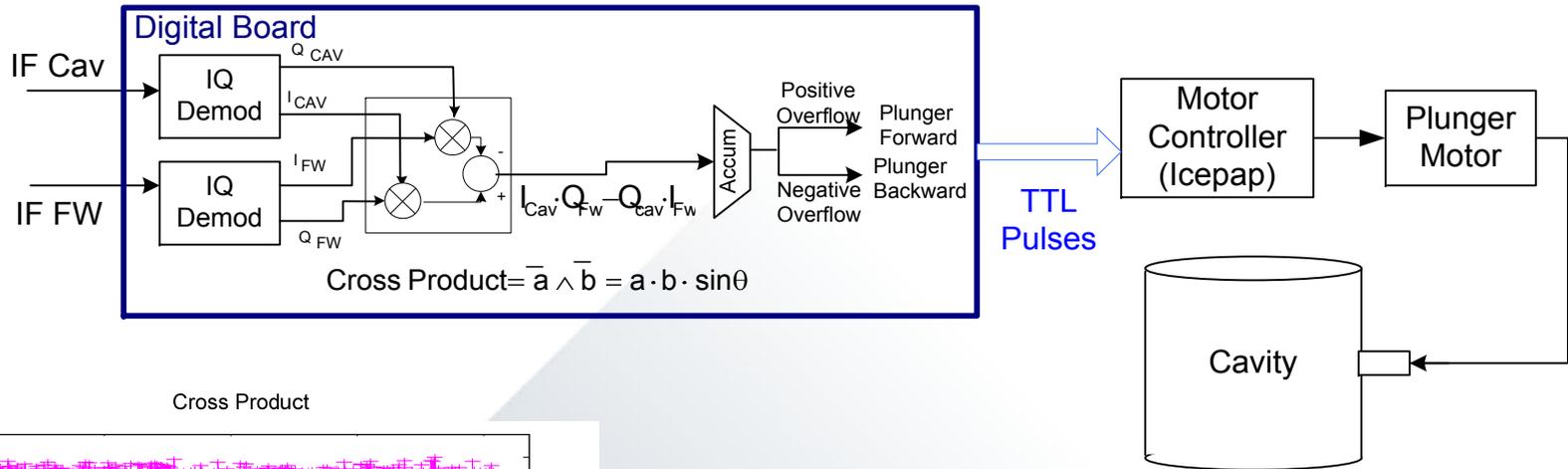
Diagnostics signals

IQ Cav
 IQ Fw
 IQ PID Output
 IQ Error

Cav Phase
 Fw Phase
 Control Phase
 IQ Integral Action

Cav Amplitude
 Fw Amplitude
 Control Amplitude

➤ Approach I: Cross Product as phase discriminator



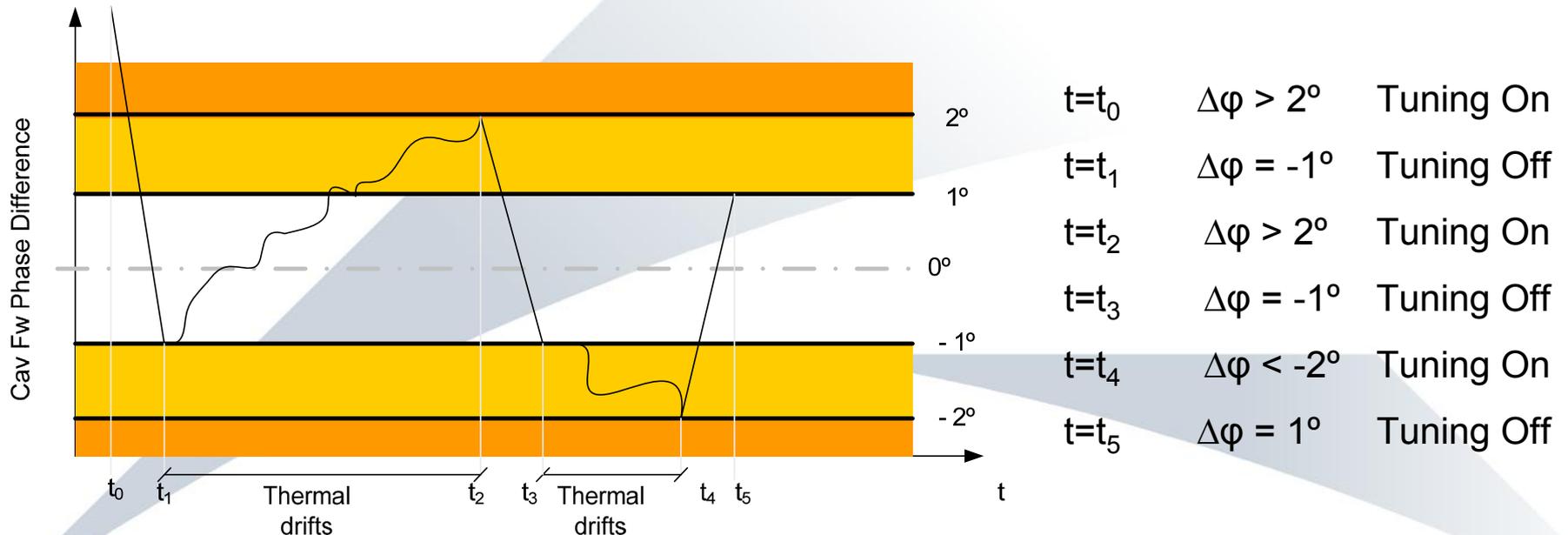
- Easy to implement, but
- Not direct measurement of Cav Fw phase
- Pulses Frequency depending on the amplitude of the Cav and Fw signals

➤ Approach II: CORDIC Algorithm to calculate Cav – Fw phase difference

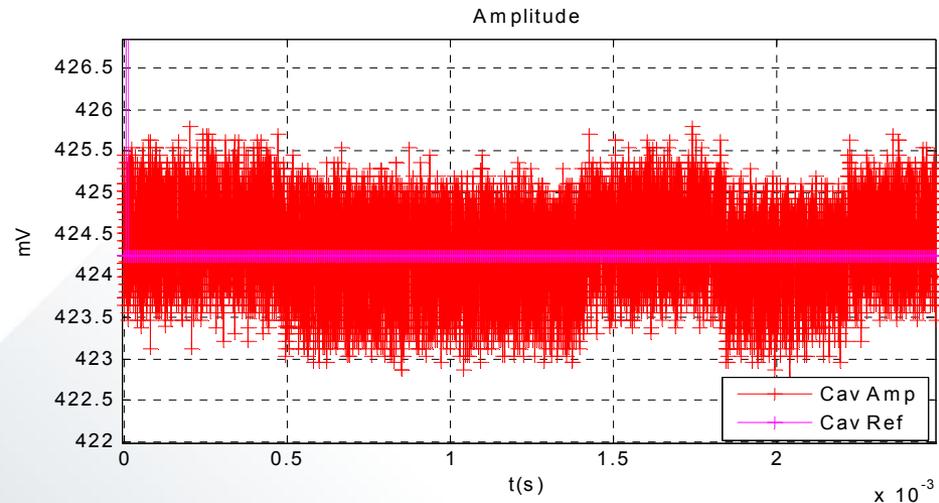
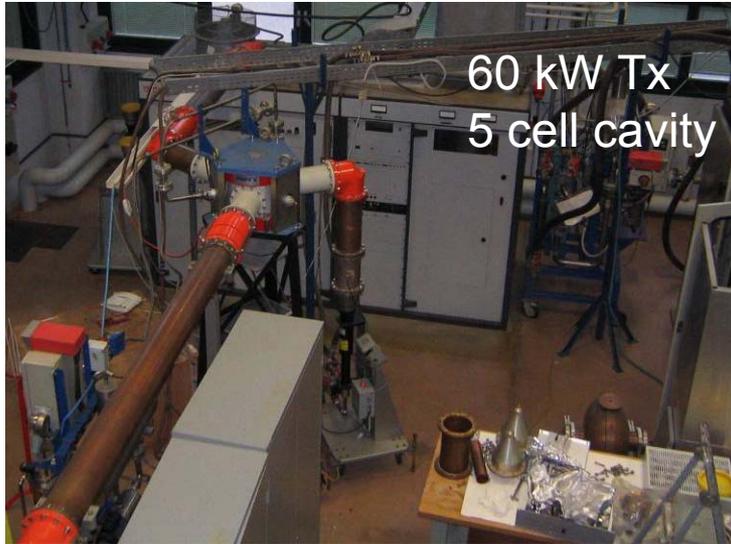
Iterative process to calculate phase without employing any multipliers

Resolution better than 0.001° after 16 iterations ($1/80\text{MHz} * 16 = 0.2 \mu\text{s}$)

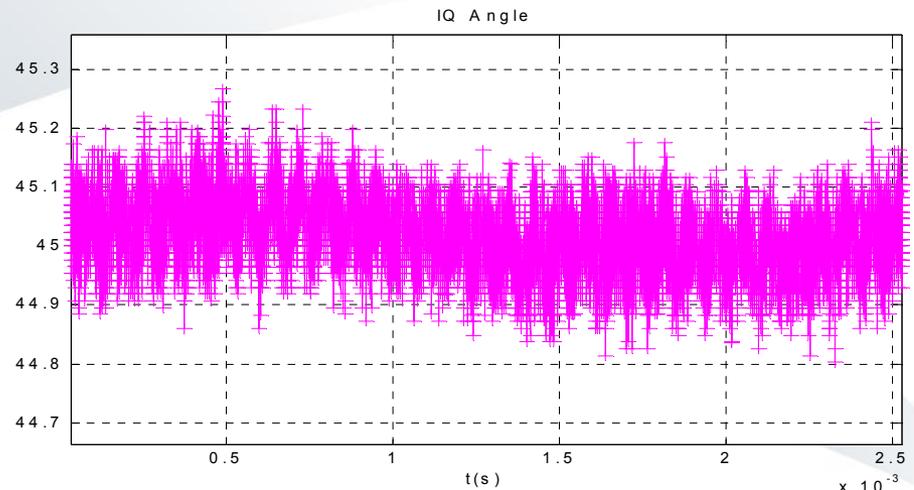
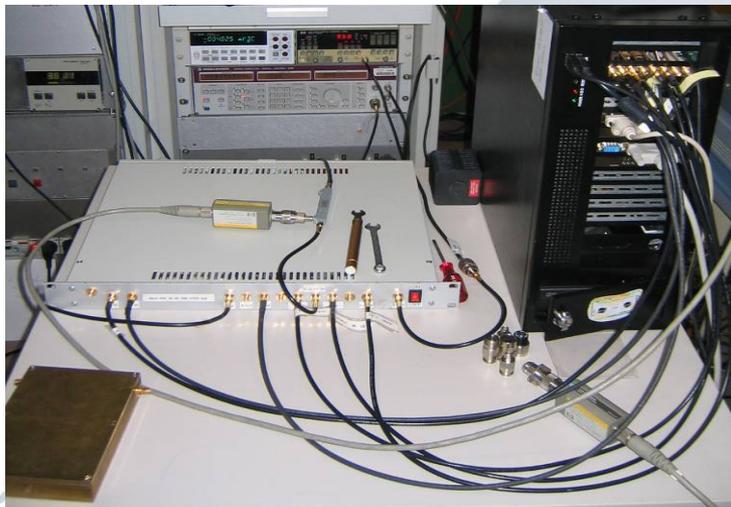
➤ Tuning Loop not always active to avoid plunger oscillations around 0° phase



Amplitude and Phase Control Loop with Sundance Board



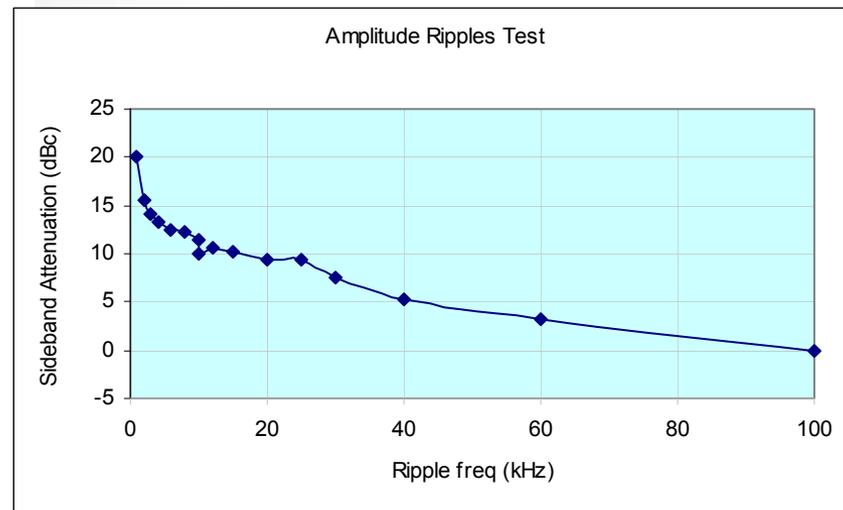
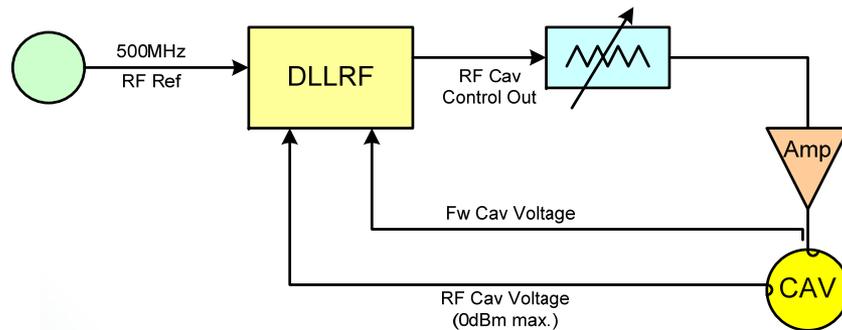
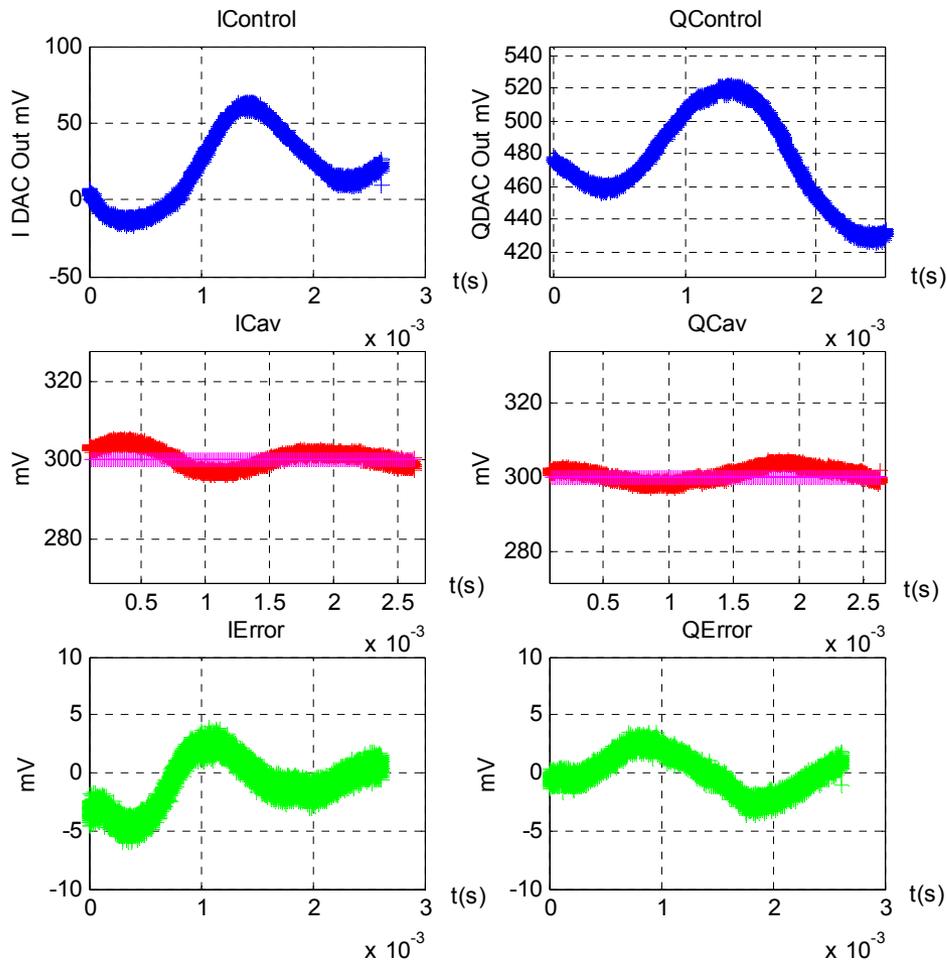
Amplitude Resolution $\pm 0.25\% V_{p-p}$ at 80MHz



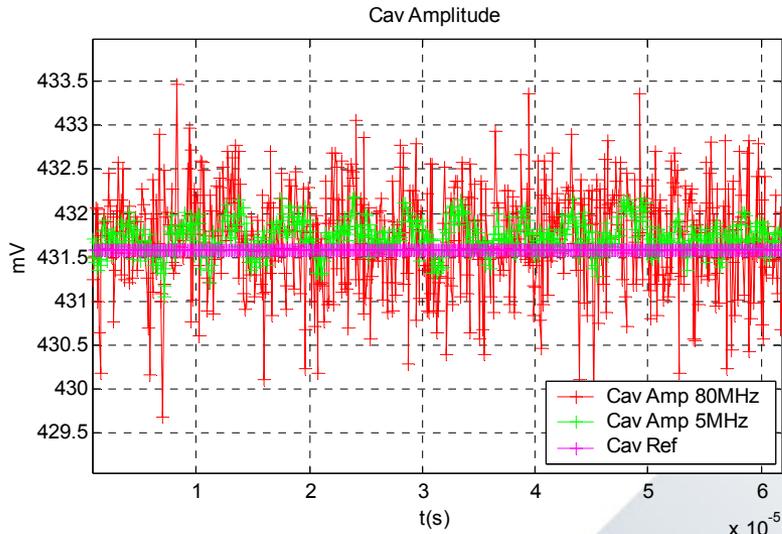
Phase resolution $\pm 0.15^\circ_{p-p}$ at 80MHz

Amplitude Ripple tests

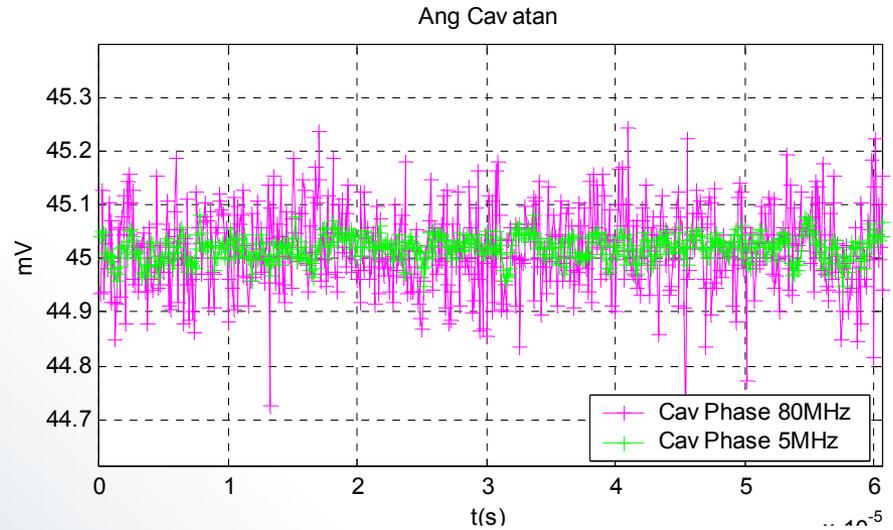
Close Loop (5kHz perturbations; 40% amplitude)



Amplitude and Phase Control Loop with Lyrtech Board

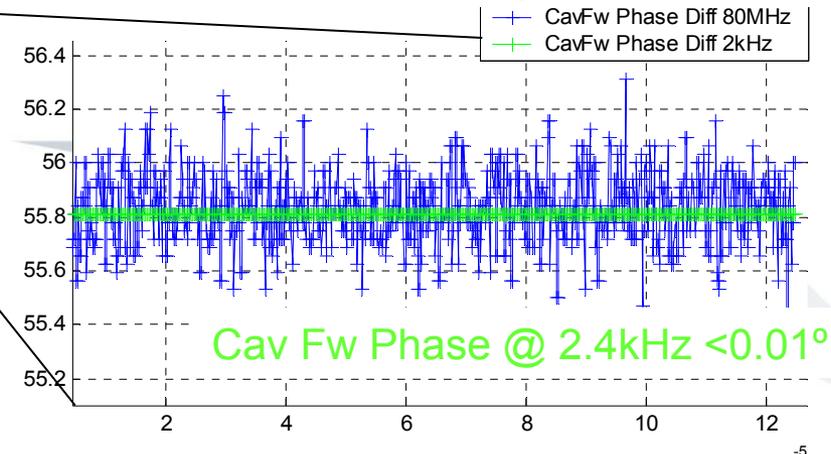
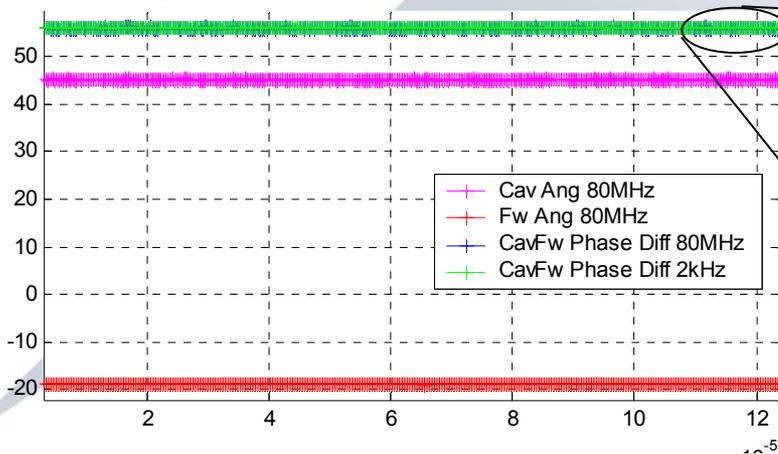


Amplitude resolution $\pm 0.3\%$ @ 80MHz
 $\pm 0.1\%$ @ 5MHz



Phase Resolution $\pm 0.2^\circ$ @ 80MHz
 $\pm 0.05^\circ$ @ 5MHz

Tuning Loop with Lyrtech Board. Phase measured with Cordic algorithm



- Amplitude, phase and tuning loops
Implemented and tested
- RF Diagnostics (15 signals)
Implemented and to real test in RF high power lab (Nov 07)
- Tender to buy Digital boards
Out in December 07
- Series production
May-June 08
- Commissioning
September 08 – March 09

Questions?

Please, only the easy ones ;-)