

OCTOBER 22-25, 2007

LLRF07

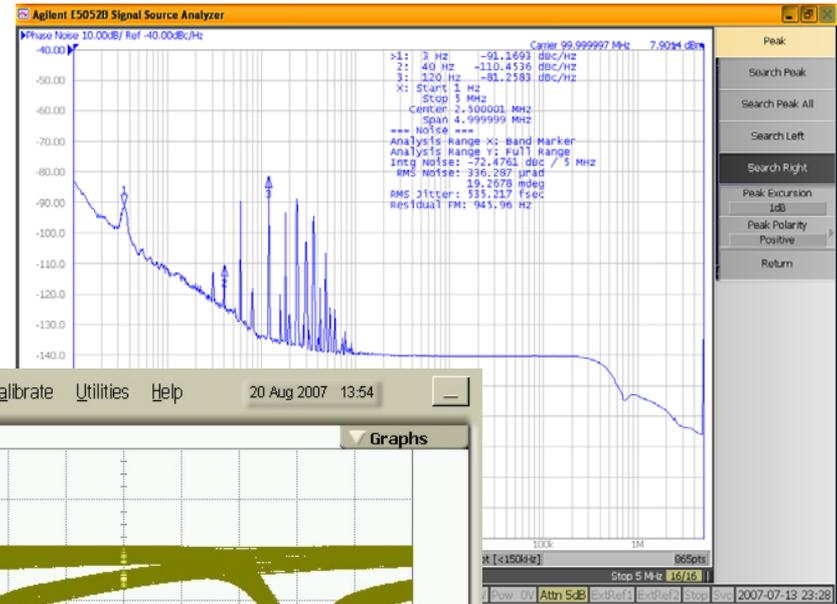
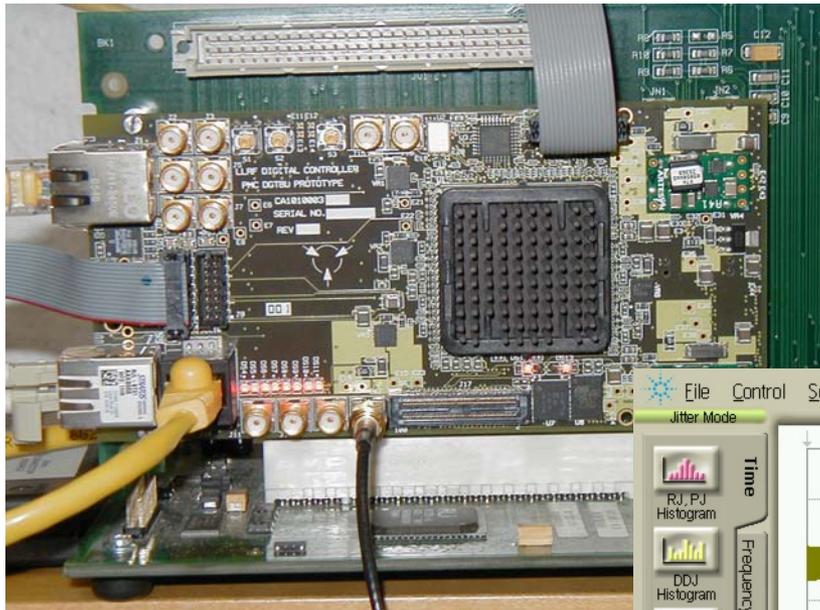
ICFA

OAK RIDGE
National Laboratory



LLRF Developments at the BNL Collider-Accelerator Department

K. S. Smith (for the C-AD RF Group)



People Involved in BNL C-AD LLRF Efforts

- RF Group Leader A. Zaltsman
- LLRF Hardware, Firmware T. Hayes, K. Smith, S. Yuan
- LLRF Software, Embedded Development F. Severino, M. Harvey
- RF Accelerator Physics M. Blaskiewicz, J. M. Brennan
- Control System Engineering L. Hoff
- Operations Machine Specialist K. Zeno

Basic Outline

- Overview of RF systems at BNL C-AD.
- Introduce the LLRF Upgrade.
- Description of architecture we have planned for the upgrade.
- What have we actually accomplished so far?
- Plans and schedule going forward.

Condensed Overview of RF Systems at C-AD

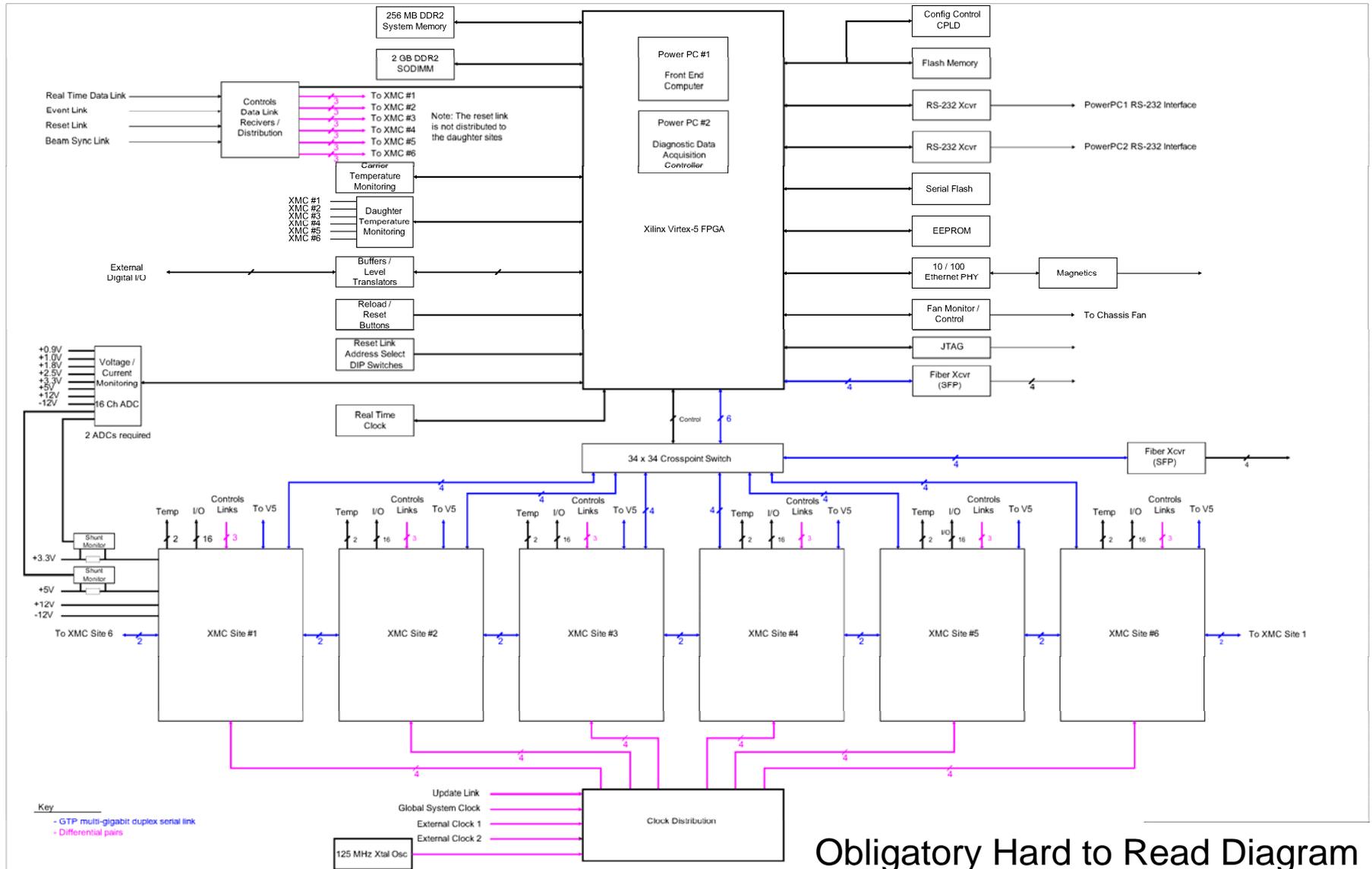
- Three primary machines: RHIC, AGS and Booster
 - Machines are all hadron rings. RHIC is a two ring collider.
 - RF frequencies ranging from 350 kHz to 197 MHz.
 - RF frequency sweeps from x10 in Booster to 0.5% in RHIC.
 - When machines run independently, require standard RF loops:
 - Cavity voltage, phase and tuning servos.
 - Beam control loops: BTB phase, radial, frequency.
 - Often require RF control of bunch gymnastics:
 - Split, merge, squeeze, debunch-rebunch, rebucketing, damping.
 - When machines are coupled require synchronization loops:
 - Booster to AGS: Machines synchro on the fly.
 - AGS to RHIC: Machines synchro at fixed field (frequency).
 - RHIC relies on ring to ring synchro up the ramp to avoid tune modulation.
 - Also require “cogging” control for bunch filling patterns.
 - PPM (Pulse to Pulse Modulation).
 - Machines multi-task species, energies, intensities from cycle to cycle.
 - 8 PPM “Users” (configurations) which must run on demand.
- New systems are coming:
 - ERL 700 MHz SCRF, RHIC 56 MHz SCRF, EBIS 100 MHz LINAC ...

The LLRF Upgrade Project

- The LLRF systems across C-AD have been developed over many years, using a variety of technologies: analog, digital, NIM, VME, PC.
- System architectures share some commonality (e.g. Booster and AGS), but also as many differences, making them cumbersome to maintain and operate.
- RHIC has the newest LLRF system at only ~10 years old. All systems are showing signs of their age and spare parts are limited.
- We have a limited number of people to maintain and operate the existing systems (all are expert systems), as well as develop new systems.
- LLRF system configurations and functionality for all machines tend to be very dynamic.
- In an attempt to satisfy the requirements of all existing and new systems, we have undertaken the LLRF Upgrade with the following goal:
 - Design a stand alone, generic, modular LLRF controller architecture which can be configured to satisfy all of the LLRF control demands we currently have, and which will be supportable and upgradeable into the foreseeable future.
 - Easy to deploy, integrate seamlessly into existing controls infrastructure, useful in other signal processing and data acquisition roles (ERL and RHIC BPMs?).

Primary LLRF Development Effort: The Controller

- A Controller is the basic building block from which a complete LLRF system is built.
 - “System Controller”: Beam control loops, synchro loops, damping, adaptive loops (cycle to cycle feedback).
 - “Cavity Controller”: Individual cavity amplitude, phase, tuning, HPRF parameters.
- Two major components from which any Controller is configured:
 - “Controller” = “Carrier” + “Daughters”.
 - Carrier Board
 - Stand alone control system interface, daughter host platform, communication hub and data acquisition engine.
 - Custom Daughter Modules
 - Provide system specific functionality via data acquisition capability and processing horsepower.
 - ADC, DAC, DSP ...
- Obviously other support modules around this (we still like NIM physical format).



Obligatory Hard to Read Diagram

Carrier Board Major Sub-Components (I: Embedded Processing)

- Xilinx Virtex-5 FXT with dual hardcore PPC440s running VxWorks.
 - PPC1: Stand alone LLRF system controller and control system interface.
 - The C-AD Controls System is standardized around VME, with MVME-2100 PowerPC FECs (Front End Computers, like EPICS IOCs) running VxWorks.
 - The PPC440 allows us to embed this functionality directly into our own hardware. MVME-2100 and VME crate and standard controls hardware not necessary.
 - Allows us to leverage the full spectrum of (existing) C-AD Controls software, and radically eases development efforts for any new software.
 - PPC2: Diagnostic data engine.
 - In all of our current systems, we are severely starved for diagnostic data, in number of observable parameters, and in acquisition bandwidth and depth.
 - Configures and controls data acquisition from daughters.
 - Several not necessarily exclusive modes:
 - » Streaming logging mode (decimated from circular buffer).
 - » Post-mortem snapshot of full circular buffer.
 - » Triggered acquisition much like a scope.
 - Interfaces with both C-AD controls network, and dedicated LLRF network if needed.

Carrier Board Major Sub-Components (II: GTP Serial Connectivity)

- GTPs offer fast (2.5 Gb/s nominal, 3.75 Gb/s maximum), point to point full duplex links.
 - Moves the complexity in connectivity from the physical PCB into the FPGA IP.
 - Two diff pairs per full duplex lane.
 - Not implying these are trivial under-takings.
 - Links are dedicated point to point. No arbitrating, no shared bandwidth and minimum latency.
 - We will start with “light-weight” Aurora links with guaranteed determinism.
 - Architecture supports other protocols such as PCIe, Serial RapidIO, SATA, Fiber Channel ...
- AD8152 digital crosspoint switch controlled by PPC.
 - 34 x 34 3.2 Gb/s crosspoint switch, non-blocking, broadcast capable.
 - Used as a configurable point to point switch matrix to provide maximum flexibility in routing of the GTP signals.
 - GTP connections to AD8152 (all links are full duplex):
 - 6 to Carrier FPGA.
 - 24 to daughter sites (4 ea. to 6 daughter sites).
 - 4 to rear panel SFPs.
- In addition, not routed through the switch:
 - There is one dedicated GTP route from the Carrier FPGA to each daughter.
 - 2 x 2ea. dedicated GTP routes between each daughter and its nearest neighbors.
 - There are four dedicated GTP routes from the Carrier FPGA to rear panel SFPs.

Carrier Board Major Sub-Components (III: Daughter Sites)

- Carrier hosts six daughter sites conforming to VITA 42.(0,2,3) XMC standard.
 - XMC adds one or two 6x19 pin high speed connectors to the PMC format, and makes the PMC connectors optional.
- All daughter sites share common generic interface to the Carrier:
 - XMC pin assignments conform to VITA 42.(2,3) for PCIe or Serial RapidIO up to four lanes.
 - 4 full duplex GTP routes from to Carrier crosspoint switch.
 - 2 full duplex GTP routes to each nearest neighbor (4 total).
 - 16 generic IOs, 8 to Carrier FPGA, 8 to Carrier header.
 - 4 generic IO diff pairs routed to Carrier FPGA.
 - 3 generic IO diff pairs, 1 ea. routed to “fares” neighbors.
 - Diff IO carrying standard C-AD controls links.
 - Diff reference clock sources from Carrier.
 - Diff RF Update Link.
 - Key RF link providing synchronous, deterministic events and data to all LLRF hardware across the complex. Later ...

Carrier Board Major Sub-Components (IV: et. al.)

- Differential clock and link distribution
 - System clock: 125 MHz, ultra-low phase noise.
 - External clock: Source selectable from external s.e. or diff ports.
 - Board clock: On board 125 MHz crystal oscillator.
 - Update Link: Global LLRF event link.
 - Controls links: Standard C-AD links (RTDL, EVENT, RESET).
- “Standard” peripherals
 - 256 MB DDR2 for PPCs, 2 GB DDR2 SODIMM for diagnostic data
 - 32 MB FLASH for both general purpose use and ethernet remote reconfiguration of FPGA
 - 2x 10/100/1000 ethernet, 2x RS-232 debug
 - I2C RTC, I2C EEPROM, I2C power, fan and temperature monitors
 - JTAG, buttons, LEDs, etc...

XMC Daughter Modules

- All XMC daughter modules will make maximum re-use of common functionality.
 - After common functionality is debugged once, engineers focus only on custom aspects of the front ends which provide the daughter specific functionality: ADC, DAC, DSP ...
 - Carrier interface already described previously.
 - Much commonality between daughter back end and carrier peripherals. Physical interfacing and IP cores for:
 - DDR2 SODIMM
 - FLASH and FPGA remote reconfiguration
 - Aurora links
 - C-AD Control links (RTDL, Event, Beam Sync)
 - LLRF Update link
 - Due to FPGA pin compatibility, daughter FPGA can be populated with Virtex-5 FXT (hardcore PPCs), SXT (DSP intensive), or LXT (general purpose).
 - Daughters can run either a hardcore PPC, a uBlaze soft core, or no processor.
 - Processor can run an O/S (VxWorks, Linux ...) or stand alone code.
 - Tremendous fabric resources in the Virtex-5.

RF Update Link Concept

- Aurora link at 2.5 Gb/s line rate, derived from RF master reference clock, carrying a fixed number of event/data frames with absolute determinism.
- Idea is to provide a global link to all RF systems which maintains synchronism between them.
 - Example:
 - 2.5 Gb/s with 8B/10B encoding => 250 MByte/s, or 125 MT/s for native 16 bit Aurora word length.
 - State machine with “Update” code first (last) in frame, then 124 more words of data, filled or padded with “Idle” codes.
 - Full streaming frame of 125 words every 1 μ s. So, 1 μ s update rate.
 - On “Update”, act on all other codes and data, e.g.:
 - Reset synthesizer phase.
 - Update synthesizer delta-F tuning word.
 - Read current phase of two synthesizers for comparison.
- Q: Maintain a separate RF master clock distribution, or derive master clock from Update Link via narrow band, low (enough) noise VCXO based PLL?

What have we demonstrated so far? The “PMC Prototype”

- Proof of principle module designed to test most of the new technologies we plan to use, and the feasibility of the embedded processor concept.
 - Xilinx Virtex-4, V4FX60-FF1152
 - V4 was new two years ago, now V5 is new (and improved), V6 on the way.
 - Embedded platform development
 - PPC405 running VxWorks as a stand alone RHIC FEC.
 - 32MB SDR SDRAM, FLASH, 10/100 Ethernet, RS-232 debug.
 - MGTs (now GTPs) on Cu and fiber.
 - 400 MHz DDR2 SDRAM (uDIMM).
 - 33 MHz / 32 bit PCI interface (no longer in the plan).
 - FPGA Development environments: Xilinx ISE, EDK and Platform Studio.
 - PCB Design Tools: Mentor Expedition, Design Capture and IO Designer.
- Board worked flawlessly on first spin.
- In about 8 weeks had successfully tested “everything”.
 - See ICALEPS07 paper: **“REALIZATION OF A CUSTOM DESIGNED FPGA BASED EMBEDDED CONTROLLER”**, F. Severino, et. al.
 - Indistinguishable from a standard RHIC FEC on the C-AD controls network.
 - Board has been serving as an embedded FEC development platform for a year now.

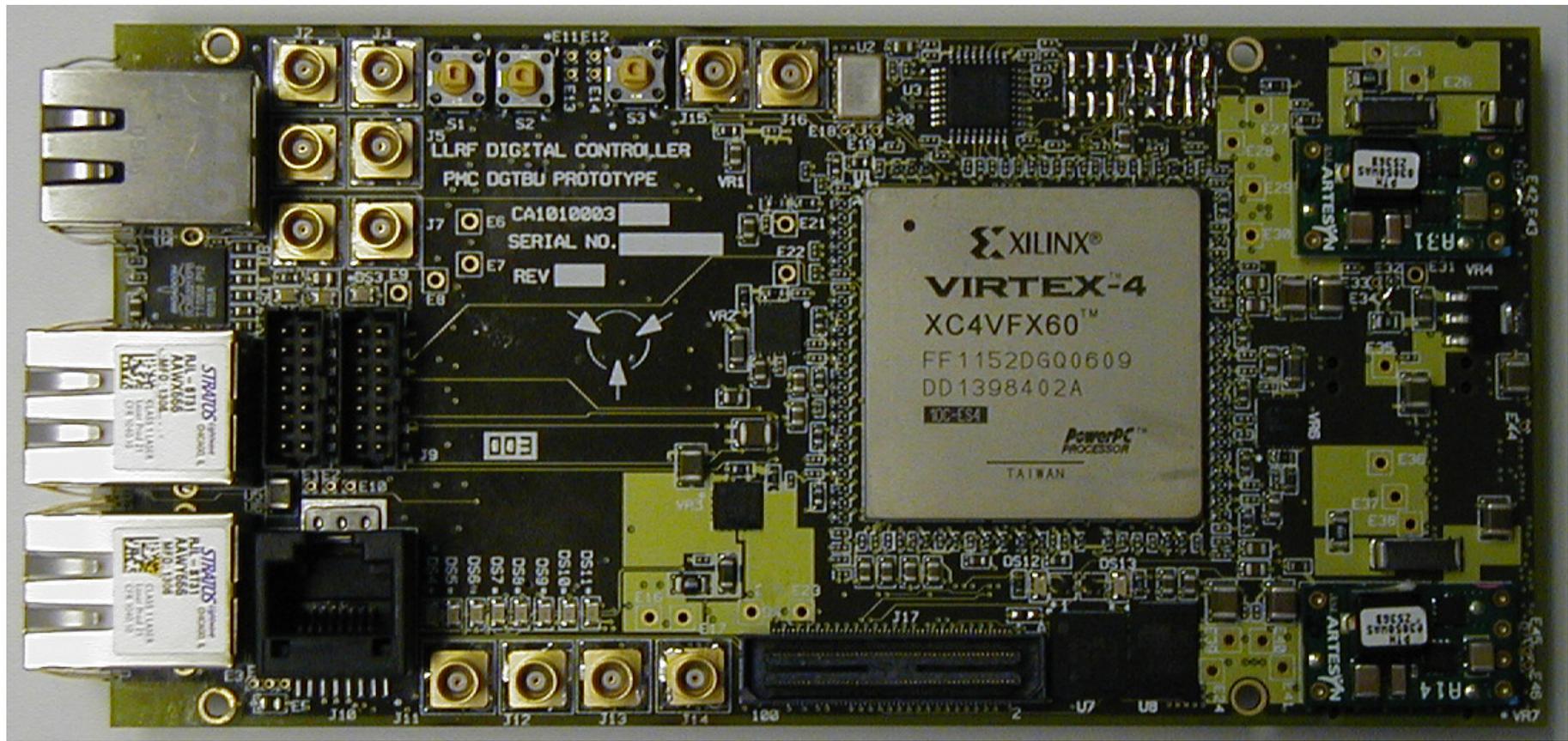
OCTOBER 22-25, 2007

LLRF07 ICFA

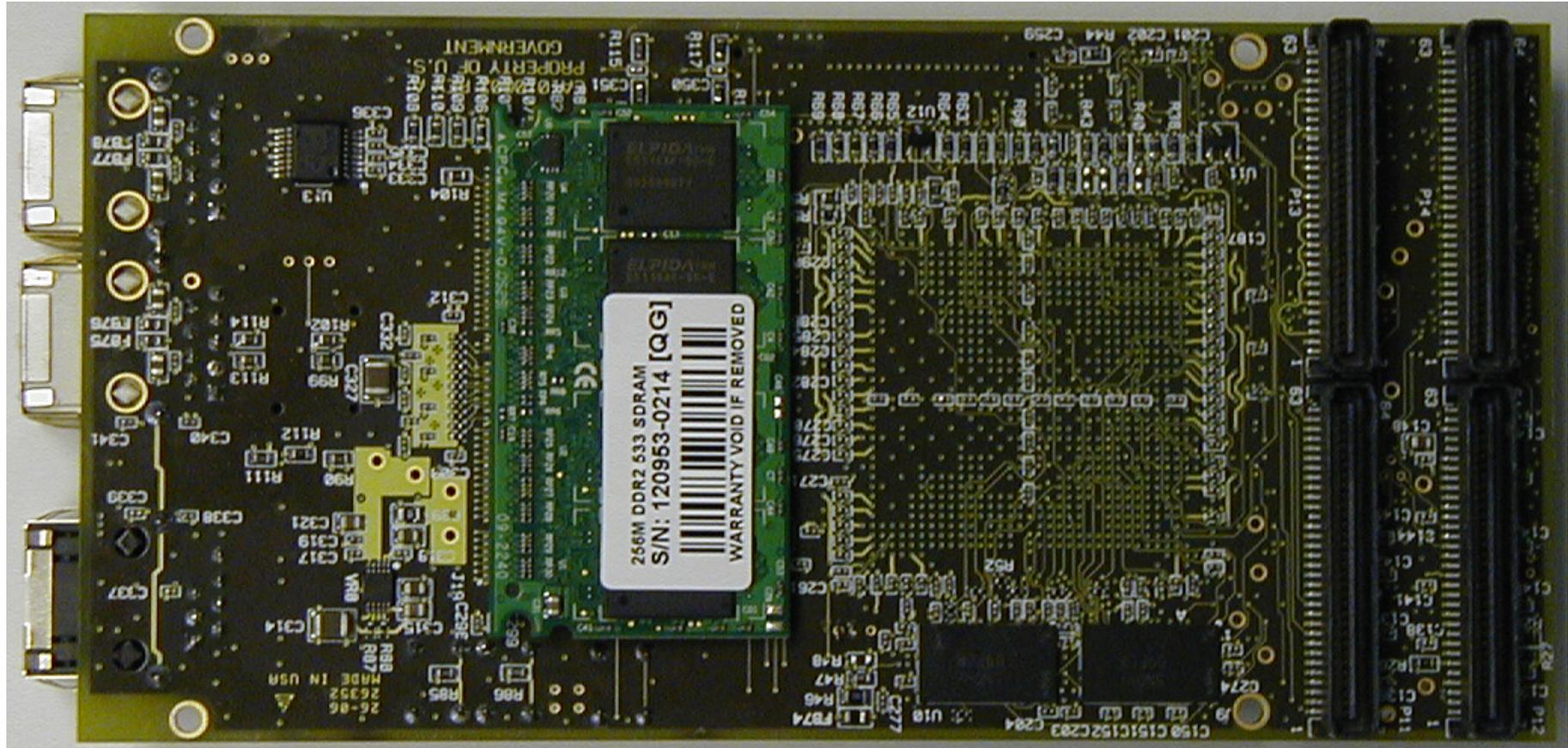
OAK RIDGE
National Laboratory



PMC Prototype Module – Top Side

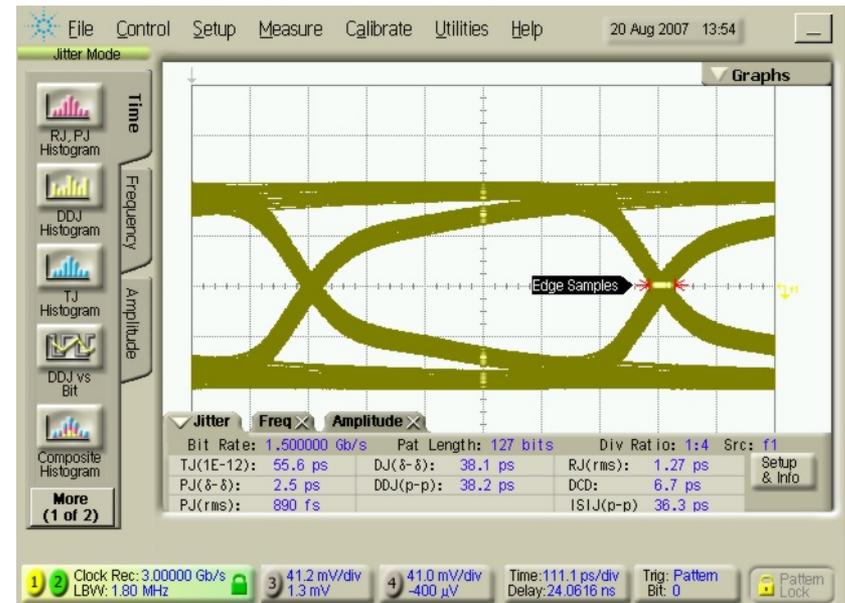
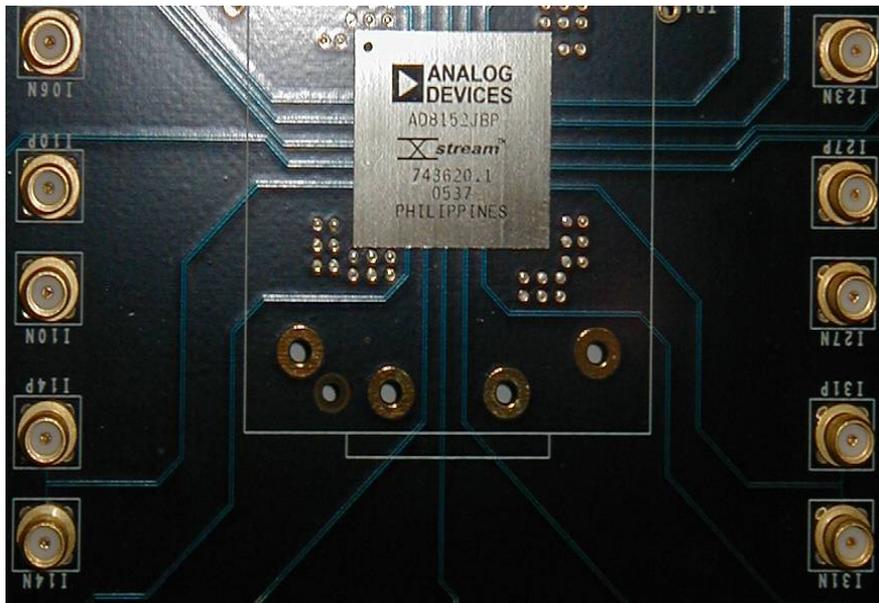


PMC Prototype Module – Bottom Side



AD8152 Crosspoint Switch

- Evaluation Board from ADI
 - Switch tested to 3.125 Gb/s using PMC Prototype MGT controlled by Xilinx ChipScope IBERT.
 - Crosstalk testing completed
 - One “clean” signal at 1.5 Gb/s. Six attacking signals, 1.5 Gb/s 7 bit PRBS (limited by Stanford CG635).



Near Term Schedule

- Best laid plans from LLRF05: “First production hardware ready in Oct 2007 (LLRF07 ?) “
- Current Effort:
 - Hardware:
 - Carrier Rev. A design complete 11/15 (T. Hayes)
 - Daughter 4CH ADC Rev. A design complete 11/15 (K. Smith)
 - Daughter 4CH DAC Rev. A design complete 12/07 (K. Smith)
 - Layout, fabrication and assembly complete 01/31.
 - Need to learn PCB design re-use tools to make this work.
 - Begin testing function cavity controller on ERL 5-cell 03/31.
 - Embedded system development continues (F. Severino, P. Harvey).
 - Firmware development starts (T. Hayes, K. Smith, S. Yuan, P. Oddo).
 - Application development starts (F. Severino, P. Harvey, C-AD controls).
 - Booster and AGS running now. RHIC starts 11/01.
 - F. Severino and P. Harvey have primary responsibility.
 - T. Hayes and K. Smith as needed.
 - RHIC mode is D/Au this year, was Au/Au last year. Impacts all machines, especially Booster and AGS setups.

Slightly Longer Term Schedule

- RHIC “Blue” and “Yellow” LLRF systems are on life support.
 - We **must** replace those systems with two operational “System Controllers” in Summer 2008, for Autumn 2008 RHIC start-up.
 - Is there time for a re-spin of Rev. A hardware?
 - Is there time to bring firmware, software to operational status?
- Reference clock distribution.
 - Need to settle on coax vs. fiber for building to building.
 - Machines also need independent clocks for autonomous running.
- Update link distribution.
 - Machines need a local hook into the update link.

OCTOBER 22-25, 2007

LLRF07

ICFA



The End

Collider-Accelerator Complex (C-AD) at BNL

