

SNS Detector Interface

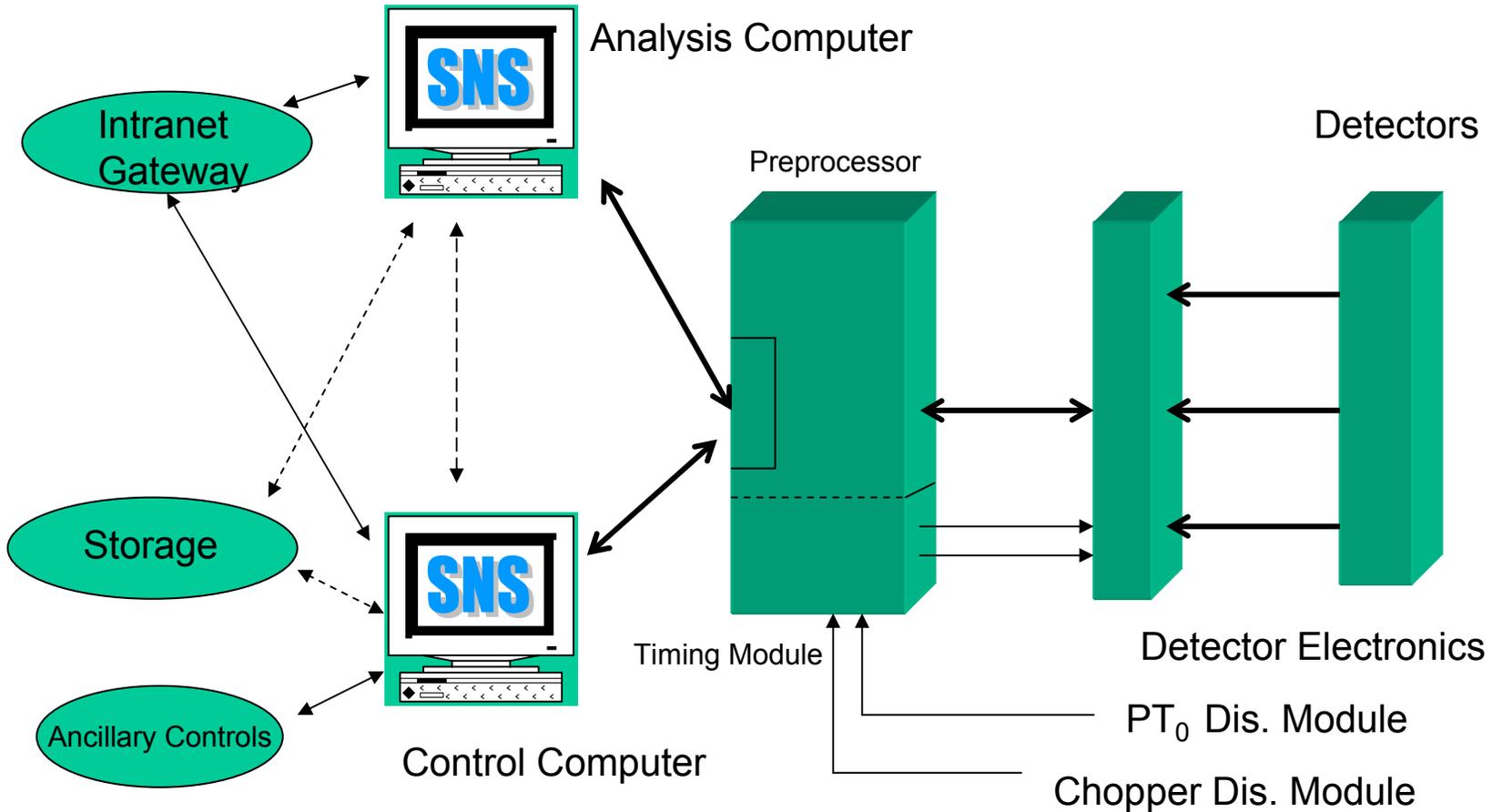
Richard Riedel
SNS Data Acquisition Group Leader

Design Requirements

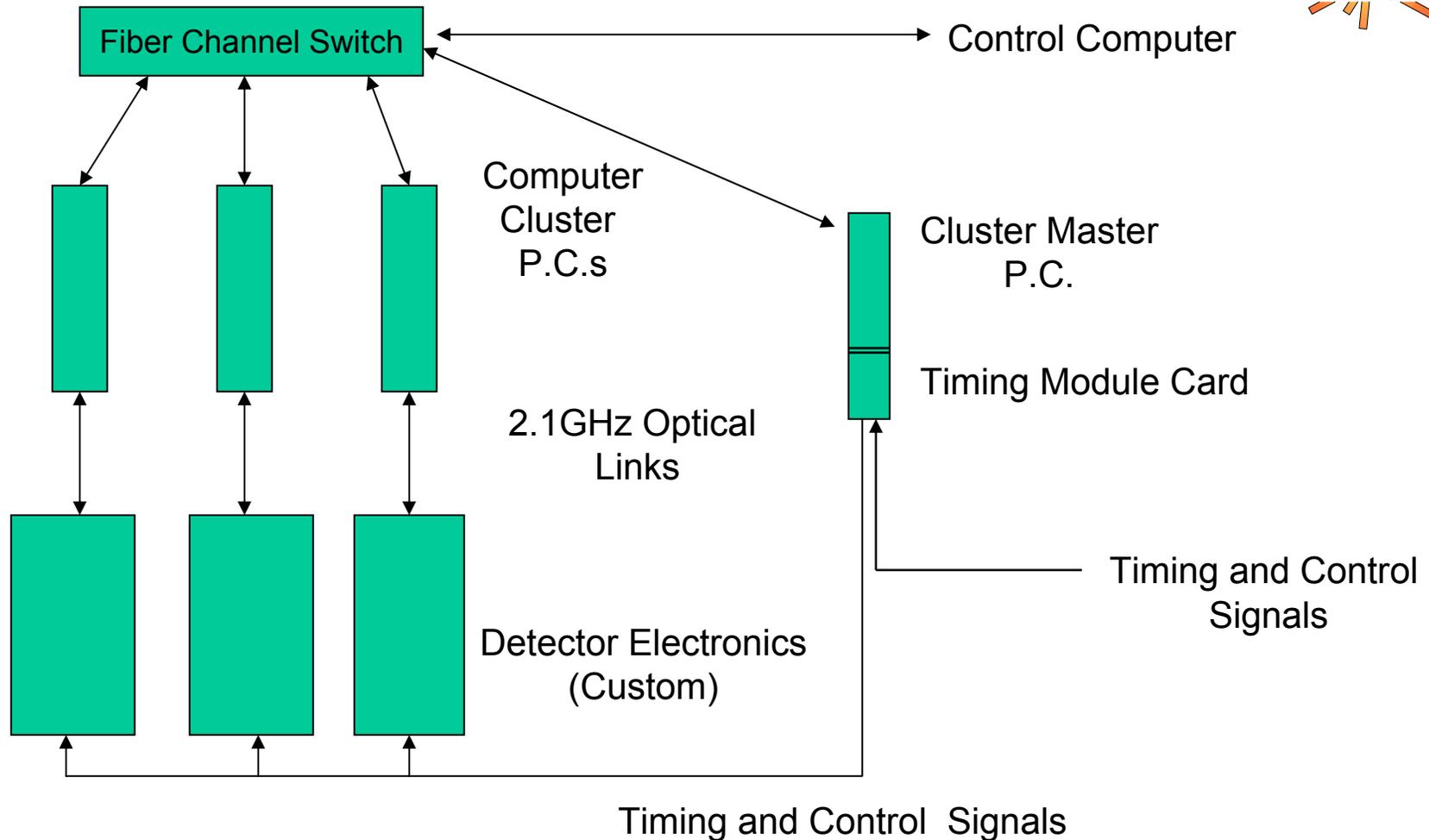


- Unified interface for all detector electronics
- Capable of “pulse” operation (individual events, no histogram)
- Data link must handle 10 million events/sec
- Architecture must be scalable.
- Galvanic isolation.
- Use of hardware address to identify components
- Must keep local copy of calibration variables.

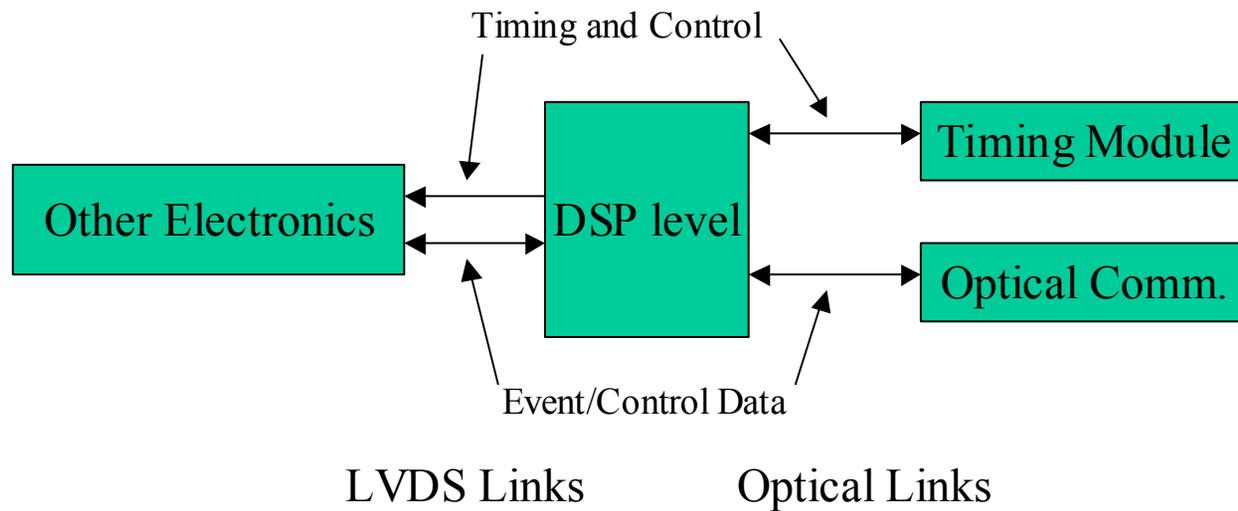
DAS System Diagram



Preprocessor Detail



Interface Link Details

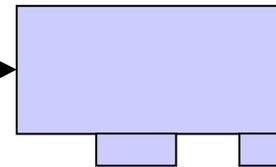


Detector Interface Components

Detector Electronics



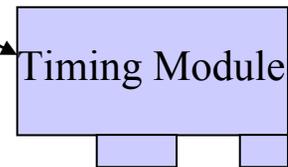
Communications Card



Fiber Links (2.1GHz)

64bit/66Mhz PCI
interface

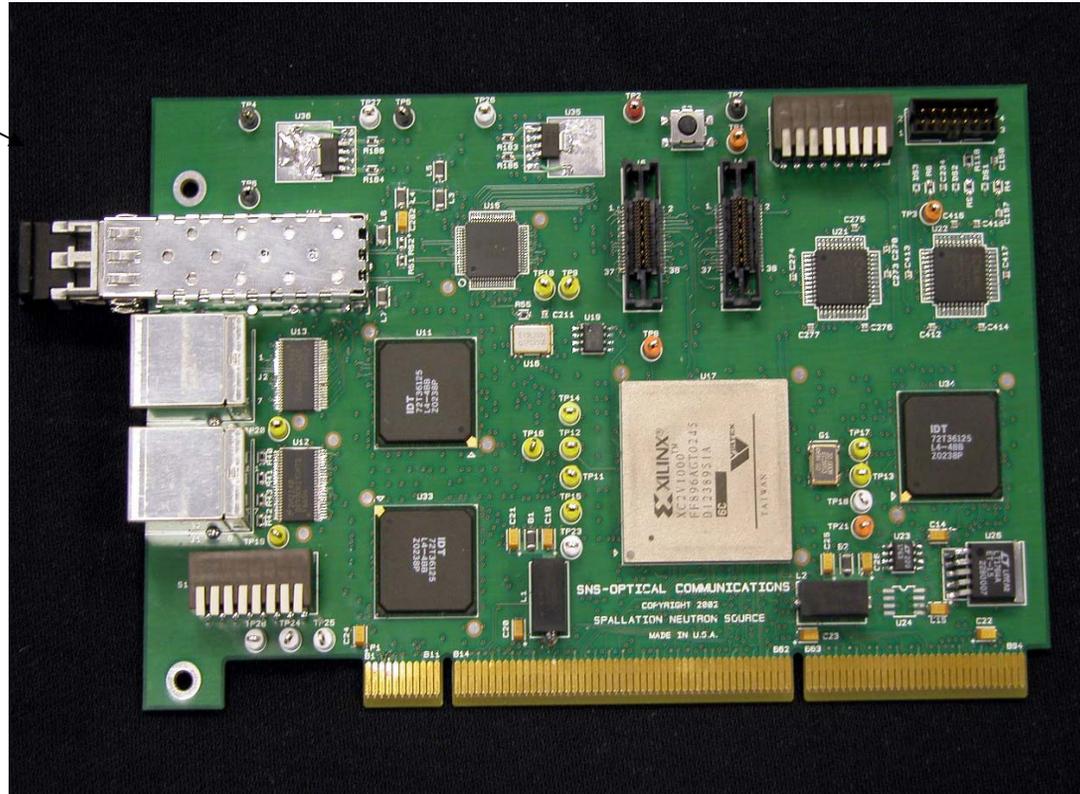
Layer 0 = Physical Interface
Layer 1 = How the bits are sent
Layer 2 = How words are packed
Higher Layers = Protocols



64bit/66Mhz PCI
interface

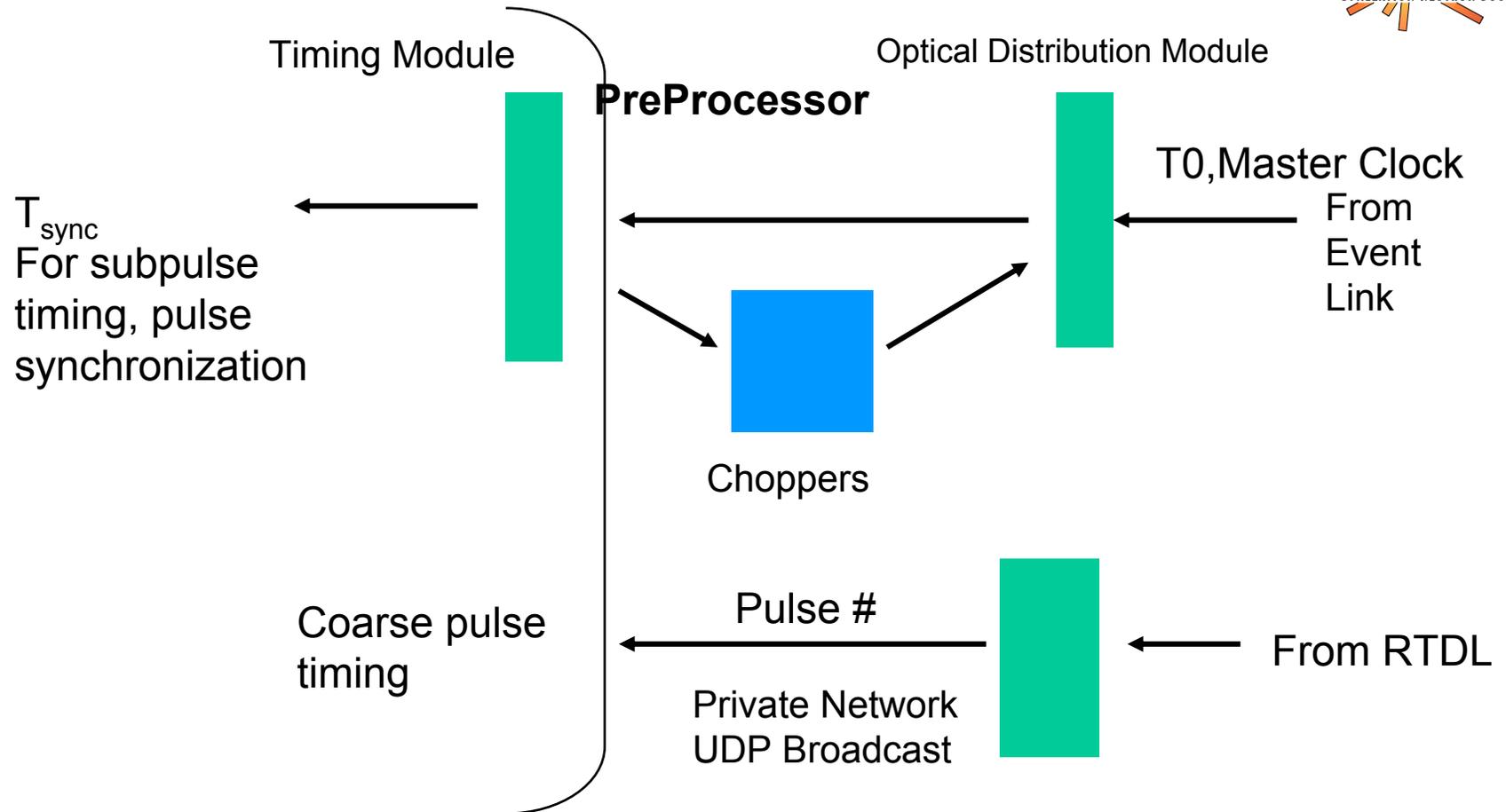
Optical Communication Card

Optical link



This card is placed in the preprocessor and receives the raw neutron data over an optical link

Timing Interfaces (per instrument)



Layers 0 and 1 Summary



- Two fiber channel links
- Type LC connector multimode fiber*
- Agilent HFBR5720 SFP

- Layer 1 protocol requires use of Texas Instruments TLK2501
- Link rate uses fiber channel speed of 2.125 GHz (requires low jitter crystal).

- Reference design available

Layer Two “Payload”



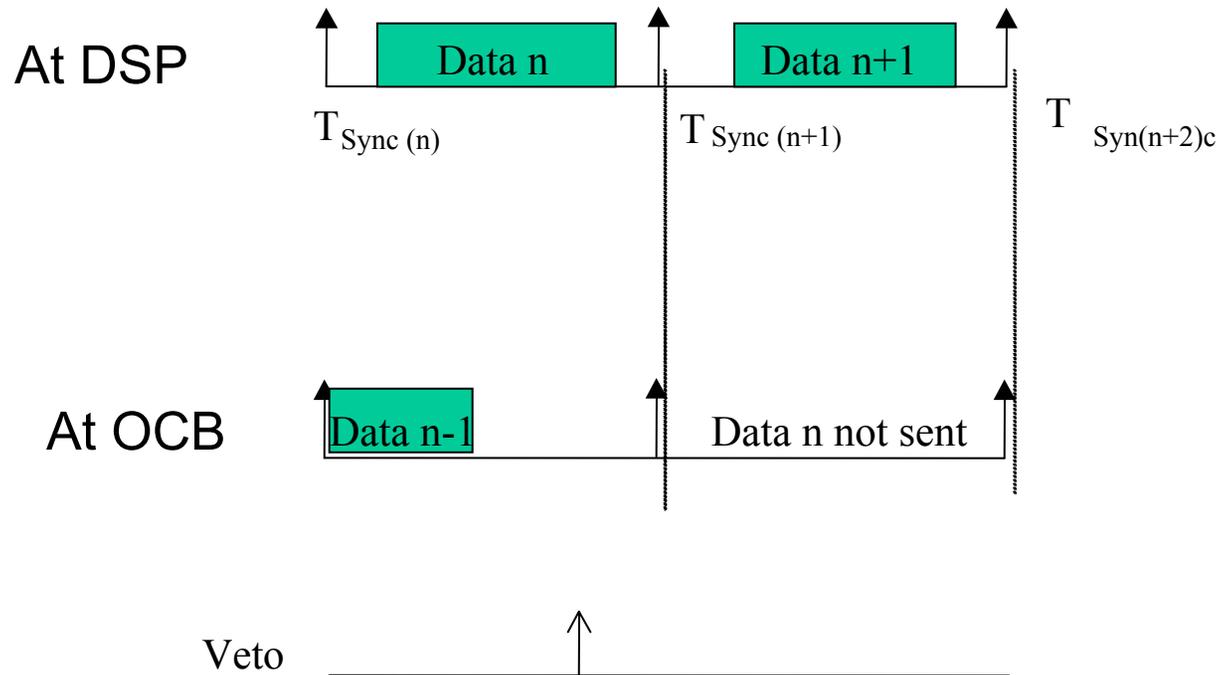
Words are 32 bits little endian

Payload is multiple of 32 bits,
limit is approximately 2Mbytes

Frame Behind Data Requirement



One frame of data must be stored in detector electronics,
it is sent only after receipt of T_{sync} without a veto



Protocol layer



- All detector electronics must support a discover command
- All detector electronics must support a 32bit unique hardware address
- All electronics are assigned a designator code by SNS for return by discover command.
- All electronics must be able to send neutron event data in the standard SNS format. (32 bit time stamp , 32 bit position stamp both little endian)

Time Stamp (32b L.E.)
Position Stamp (32b L.E.)

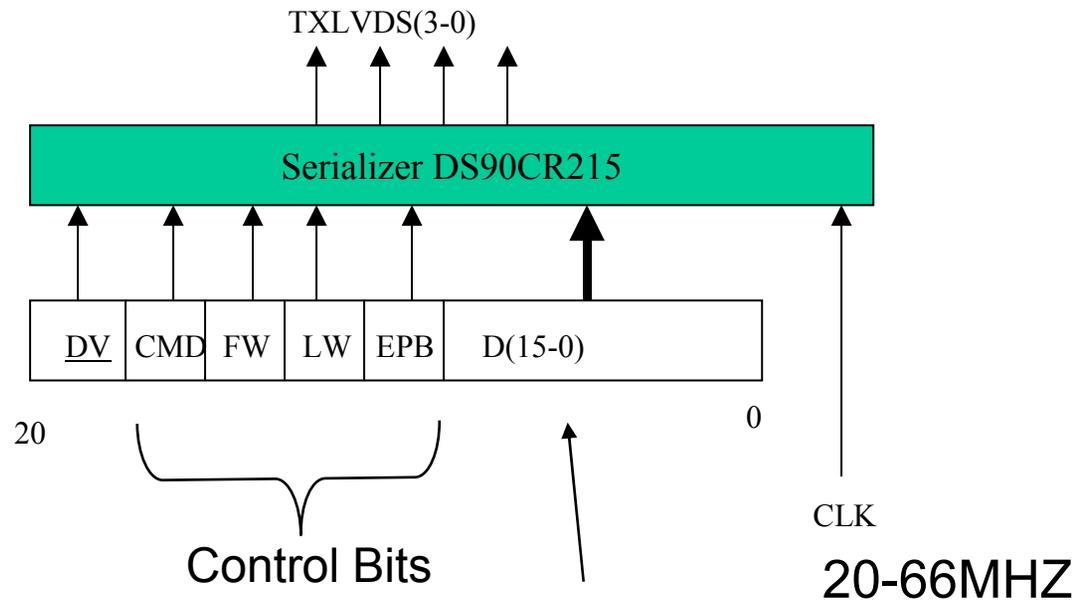
LVDS Copper Links



- May be the best choice for some applications
- Useful for testing prototypes at the ROC level
- Need three CAT 5 patch cables, two for data and one for timing and control.
- Data rates between 40 and 130 Mbytes/sec depending on detector.
- With SNS NIM interface boards can be used with National Instruments DIO Hs 32 boards.

LVDS data link.

Operates over CAT5=Physical Interface

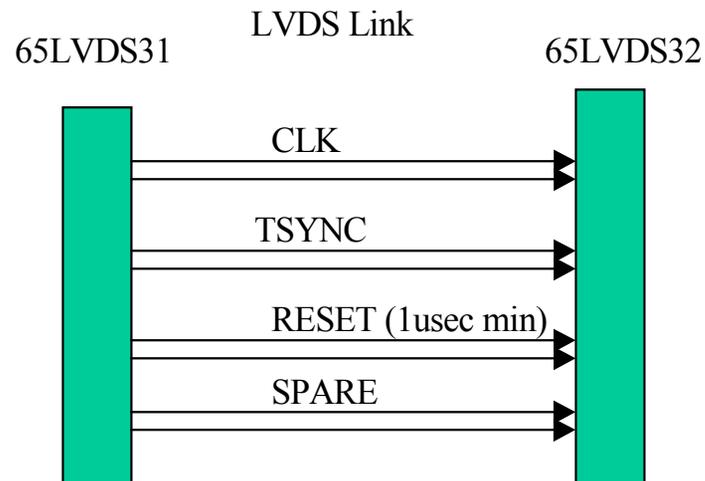


Data always sent
Little Endian Format!

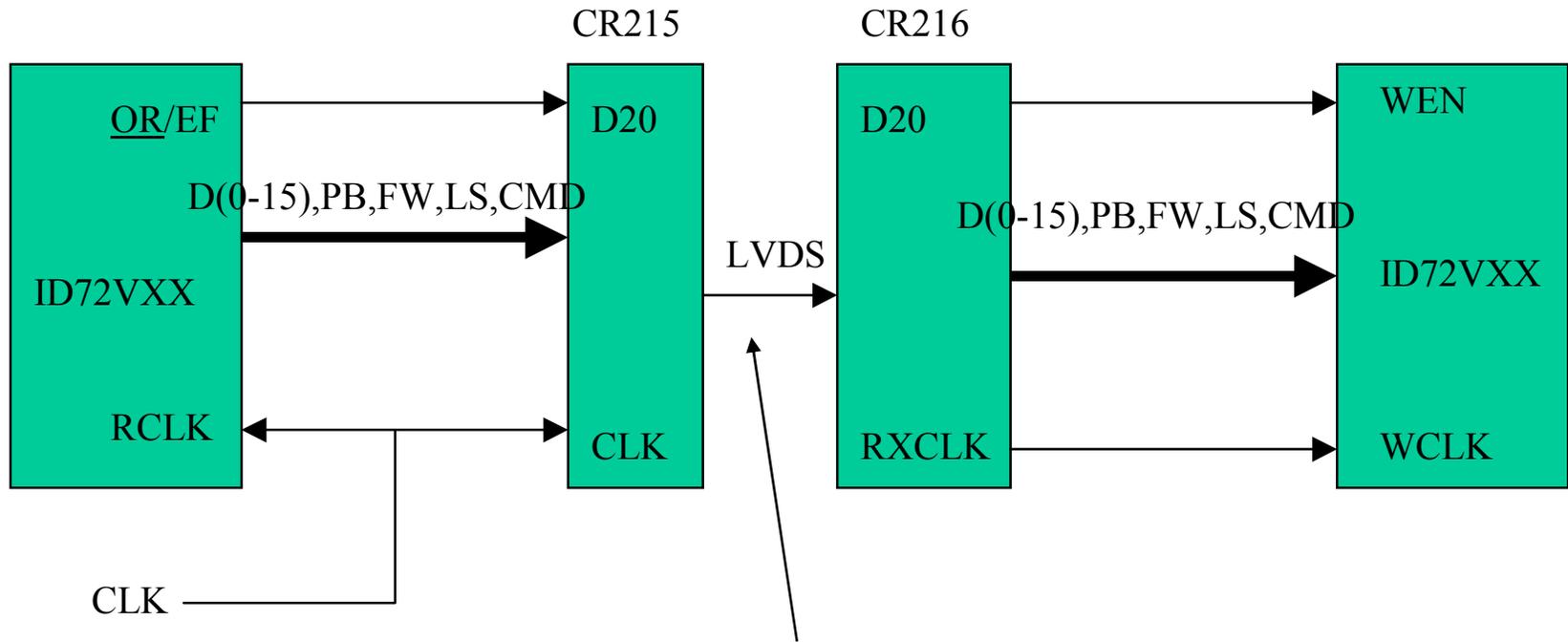
LVDS Timing and Control Interface



Operates over CAT5=Physical Interface



Coupling FIFOs is Easy



RJ45 cat 5 patch cable

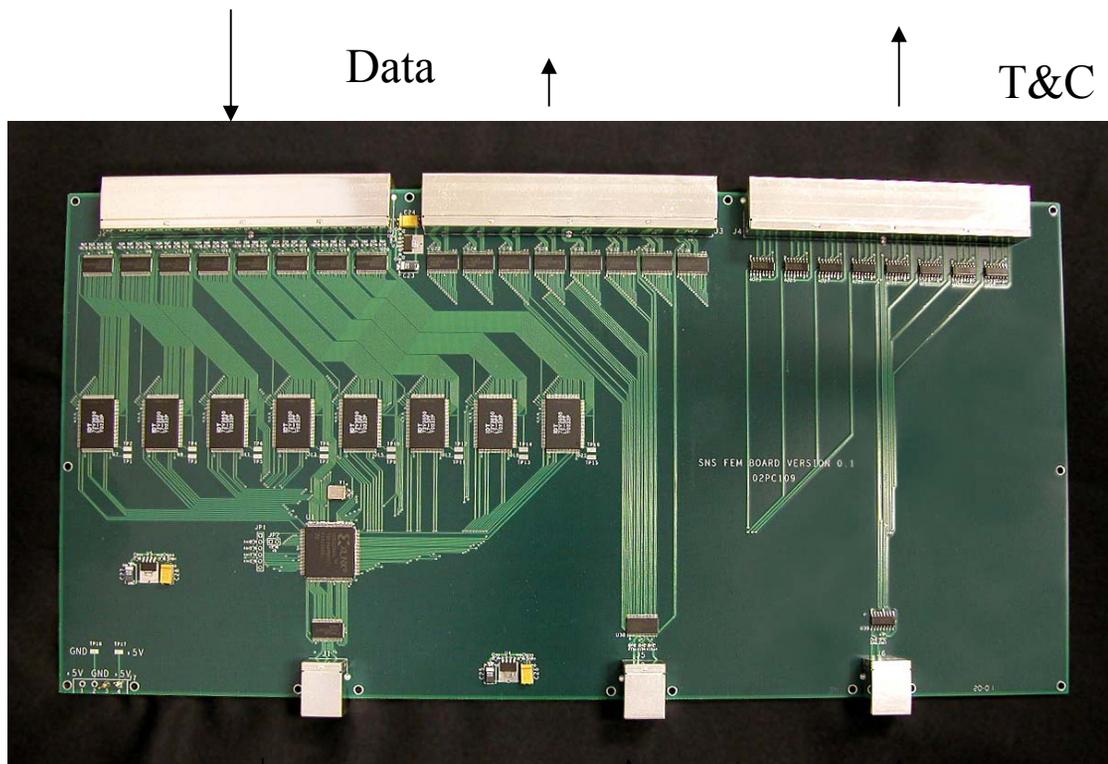
FEM Module ...Lots of RJ45

to/from ROC

Data

T&C

Analogous to
an LVDS hub

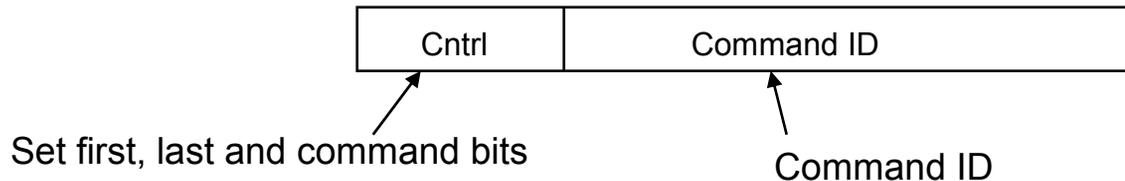


to/from DSP

Concentrates data from eight ROCs into a
single data stream. Fans information from
DSP to eight ROCs.

LVDS Layer 2 (Packets defined by first and last word bits)

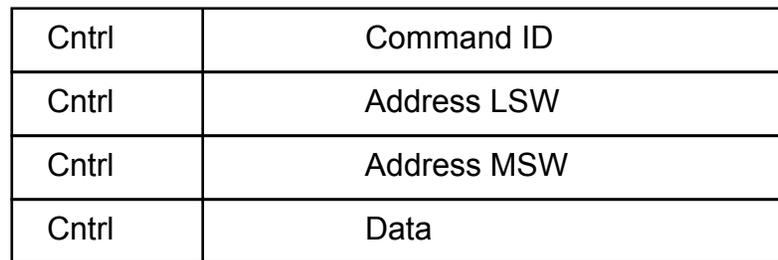
Type 1 (global)



Type 2 (addressed)

Set first and command bits

*Command responses have command bits set for all words.



A diagram showing a sequence of four packets. Each packet is a horizontal rectangle divided into two sections: 'Cntrl' on the left and a specific field on the right. The fields are: Command ID, Address LSW, Address MSW, and Data. An arrow from the text 'Set first and command bits' points to the 'Cntrl' section of the first packet.

Cntrl	Command ID
Cntrl	Address LSW
Cntrl	Address MSW
Cntrl	Data

Set last bit on last word



A diagram showing a single packet structure. It consists of a horizontal rectangle divided into two sections: 'Cntrl' on the left and 'Data' on the right. An arrow from the text 'Set last bit on last word' points to the 'Cntrl' section.

Cntrl	Data
-------	------

LVDS Layer 2



Type 3 (data)

Set first word bit

*note that command bit is never

Set last bit on last word

Cntrl	TimeStamp LSW
Cntrl	Time Stamp MSW
Cntrl	Position Stamp LSW
Cntrl	Position Stamp MSW
<hr/>	
Cntrl	Position stamp MSW

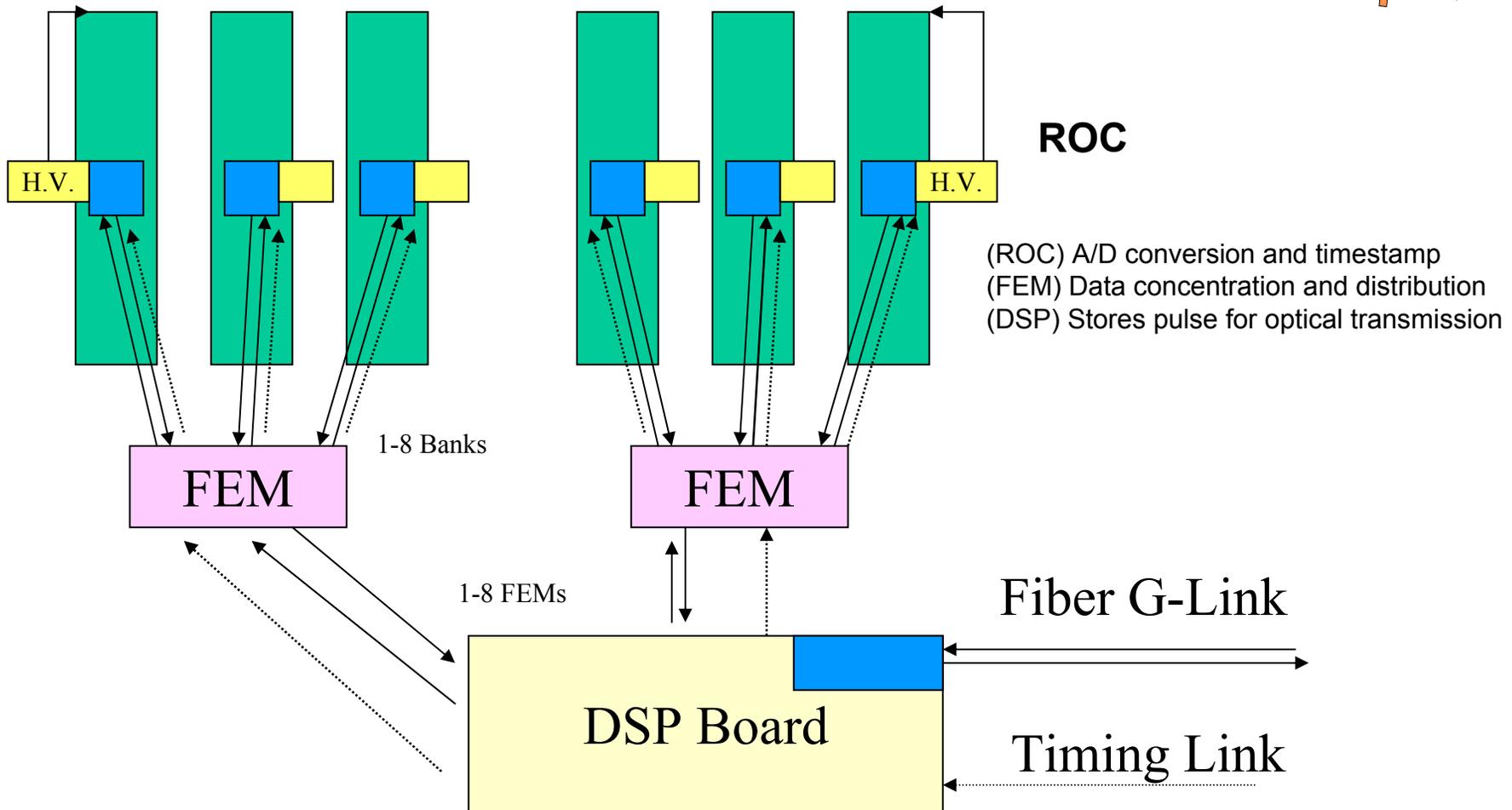
Other formats possible. !

Protocol Layer

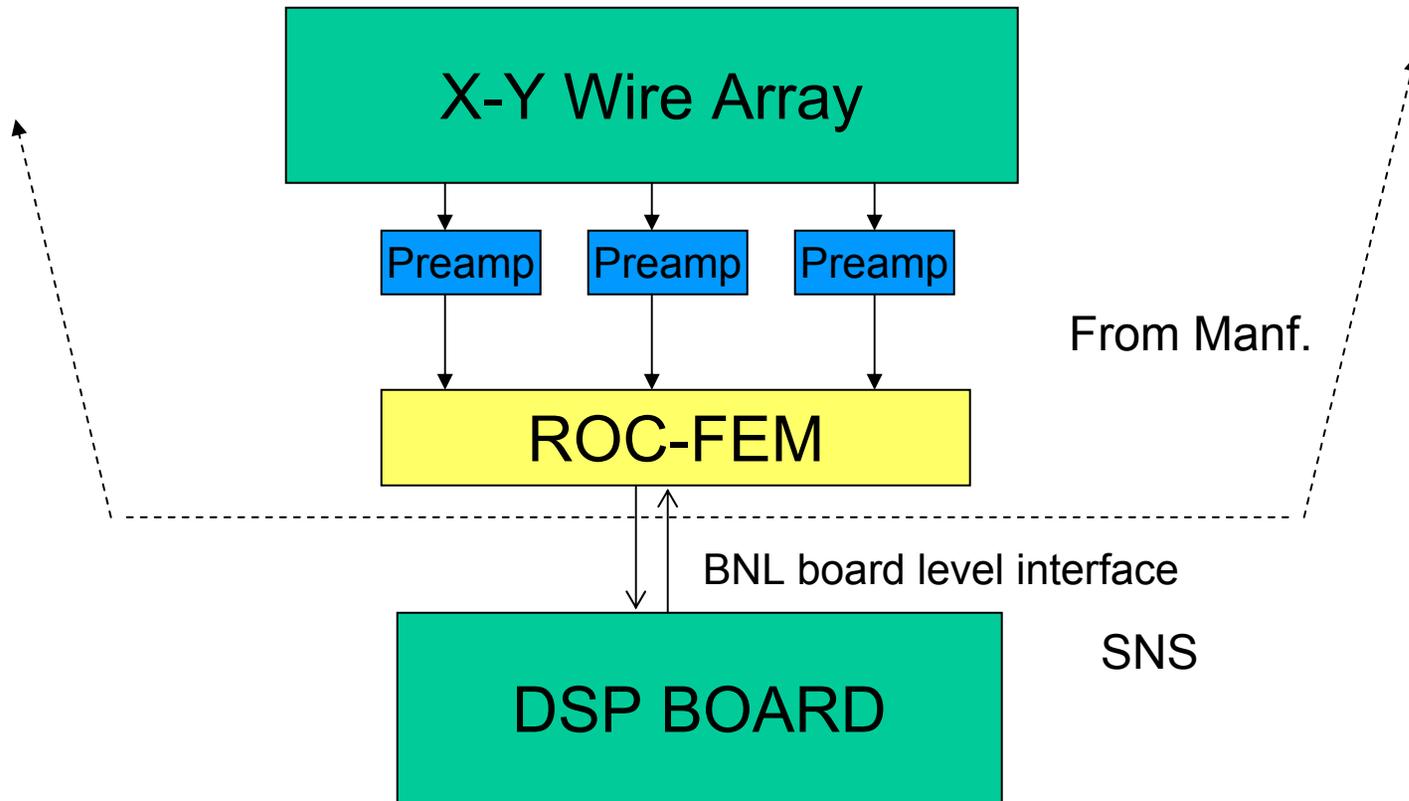


- Mirrors requirements of optical protocol.
- Must support discover
- Must support global start and stop.
- Must support hardware I.D.s
- Must support standard neutron event format.
- Typically would also support configuration and status queries.

Full Detector Array (He3 Tubes)



X-Y Detectors (Brookhaven, Orдела)



Key Features of Detector Electronics



- Makes use of high speed Field Programmable Gate Arrays (FPGA) which are 10 – 1000 times faster than Digital Signal Processors (DSP).
- Use of common FPGA platform
- Verilog Hardware Description Language (VHDL) code reusable between various parts of the design
- New code downloadable via preprocessor links
- Position calculations can be done at ROC level.*

Eight Up Detector Bank

