

Front-End Electronics

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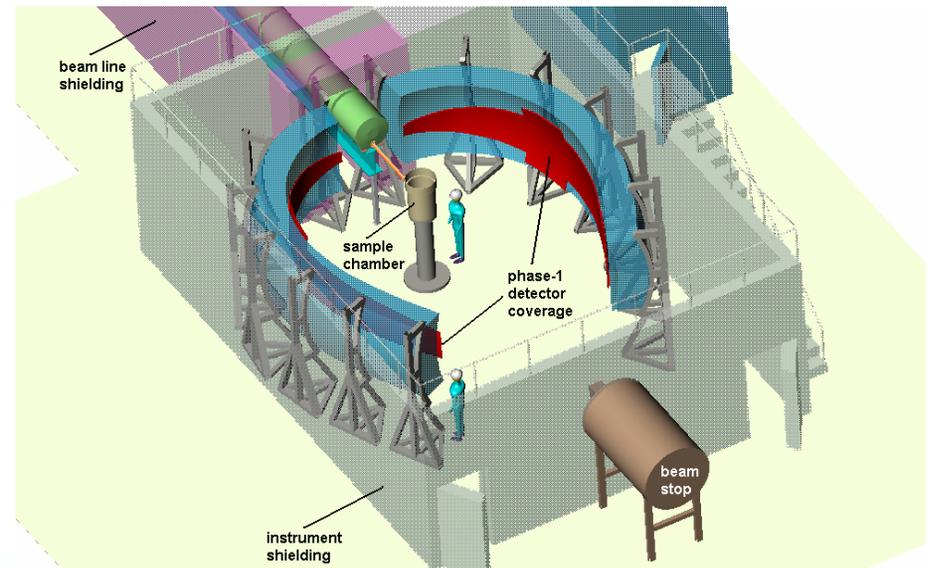
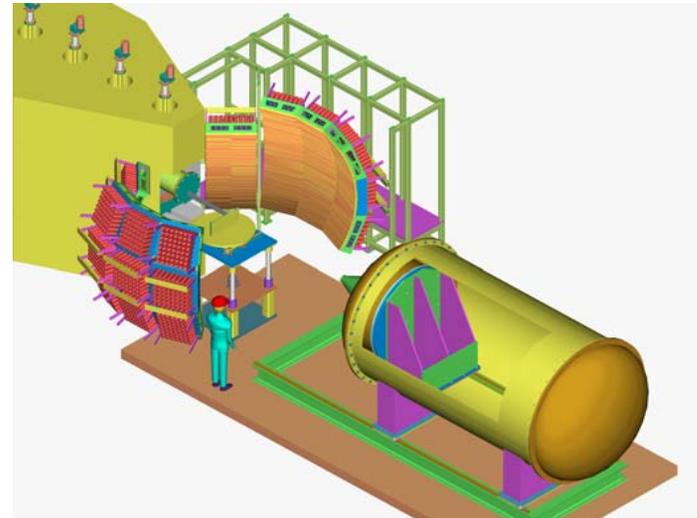
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**Presented at the Indiana University Neutron Detector Workshop
May 29, 2003**

We'll discuss....

- Why Custom Application-Specific Integrated Circuits (ASICs)?
- Custom ASICs 2-page tutorial
- Pixel Detectors
- Challenges abound



SNS Pixels as of 2000



Desired Parameters for the SNS neutron scattering instruments. (Apr 2000)

Parameter	Backscat. Spect.	Magnetism Reflect	Liquids Reflect.	Powder Diff.	Single Xtal Diff.	Chopper Spect.	Disord. Mat'ls Diff.
Spatial pixel area (cm ²)	1	0.01	0.01	1.2	0.01	6.25	1.2
Total # of pixels	7,000	10,000	10,000	170,000	5,000,000	50,400	150,000
Minimum time of flight (microsec)	50,000	2,400	1,800	4,000	1,000	800	250
Maximum time of flight (microsec)	150,000	96,000	73,000	100,000	16,000	16,000	14,000
Time of flight precision (microsec)	1	10	10	0.5	1	0.2	0.2
Max # of time channels	8,400	1,500	1,500	60,000	1,000	2,000	1,000
Max instantaneous rate/pixel (cts/sec)	4,000	1.3 x 10 ⁶	1.30 x 10 ⁶	40	3.8 x 10 ⁴	30,000	2,000
Max total instantaneous rate (cts/sec)	3 x 10 ⁷	1.2 x 10 ⁸	1.2 x 10 ⁸	1.4 x 10 ⁶	1.7 x 10 ⁷	1.5 x 10 ⁹	8.4 x 10 ⁷
Max time-average rate/pixel (cts/sec)	12	6.2 x 10 ⁵	6.2 x 10 ⁵	4	2.8	4	360
Max total time-average rate (cts/sec)	8.5 x 10 ⁴	5.9 x 10 ⁷	5.9 x 10 ⁷	1.4 x 10 ⁵	1.4 x 10 ⁷	2.0 x 10 ⁵	1.6 x 10 ⁷
Minimum time per data set (sec) *	120	1	1	120	120	120	60
Typical time per data set (sec) *	900	60	60	1,200	1,200	1,200	1,000
Total # of channels per data set *	5.9 x 10 ⁷	1.5 x 10 ⁷	1.5 x 10 ⁷	1.0 x 10 ¹⁰	5 x 10 ⁹	1.0 x 10 ⁸	1.5 x 10 ⁸
Typical # of channels per data set *	6 x 10 ⁷	7 x 10 ⁶	7 x 10 ⁶	3 x 10 ⁹	1 x 10 ⁹	5 x 10 ⁷	8 x 10 ⁷
Total # of counts per data set *	7.7 x 10 ⁷	3.5 x 10 ⁹	3.5 x 10 ⁹	1.2 x 10 ⁸	4.3 x 10 ⁹	2.4 x 10 ⁸	3.0 x 10 ¹⁰

Why custom ASICs?

If you're going to build $\sim m^2$ detectors for imaging with potentially hundreds of thousands to millions of channels to read out, it should be obvious....



There's no other economical way!

Economics take many forms.

- Space - Size of a desired pixel vs. size of readout circuit
- Power - Power density and total amount of power required per pixel
- Performance - How close can you get the preamplifier to the pixel?
- Wiring plant out of the detector - Can you combine / sparsify signals right at the detector to minimize signals coming out
- Power lines into a detector - How many different power supplies are needed?

And of course....

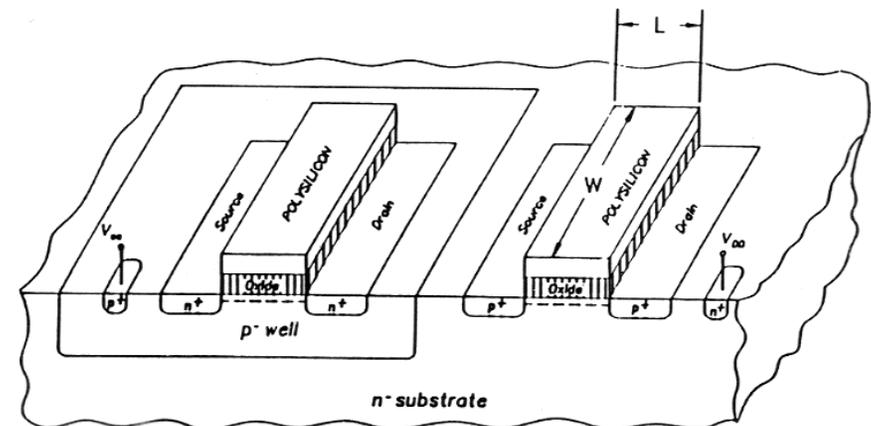
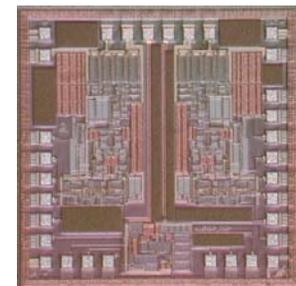
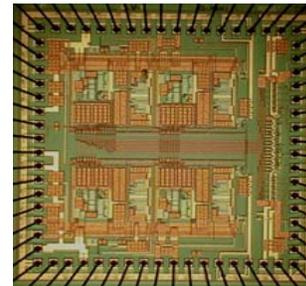


How much does it cost?



Custom ASICS 2-page tutorial

- Most ASIC design is done in CMOS (Complementary-Metal-Oxide-Semiconductor)
- Today's CMOS is actually IGFET (Insulated Gate Field-Effect Transistor)
- 'Feature size' is minimum available gate length ('L') – SOA is $<0.1\mu\text{m}$
- Commonly used feature sizes in physics are
 - $0.5\mu\text{m}$ (5V)
 - $0.35\mu\text{m}$ (3.3V)
 - $0.25\mu\text{m}$ (2.5V)
 - $0.18\mu\text{m}$ (1.8V)
- 'Bulk' CMOS popular but SOI, SOS faster, better for some applications
- Usually 3 or more levels of metal



On-chip components available

Actives – Diodes, bipolars, SiGe bipolars

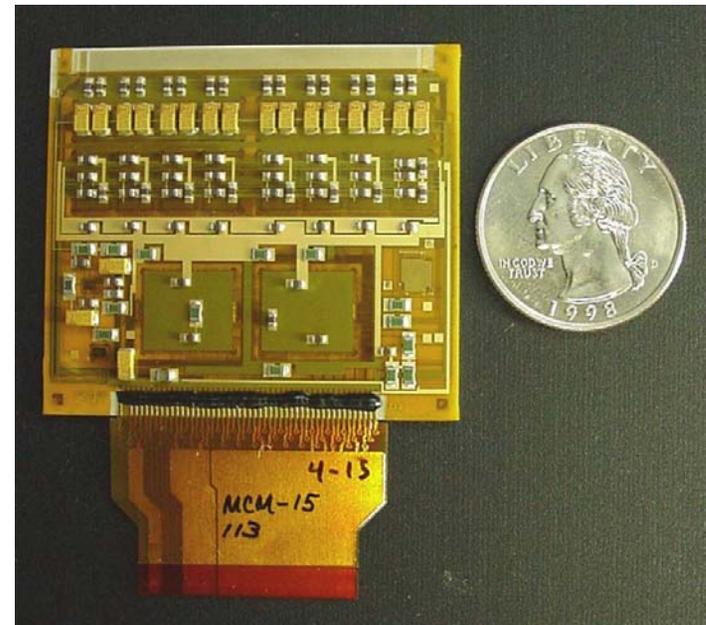
Passives – Capacitors, resistors, inductors

Custom ASICS 2-page tutorial (cont.)

- The design / fab cycle is as follows -
 - Design/simulation/layout is performed
 - Prototyping is done rather cheaply through fab brokers or with engineering runs through the target foundry (a few \$K to \$10K's for 25 or so chips)
 - After testing and verification and possibly refab, reticle is assembled for production
 - After fab, chip testing can be done at wafer level or post-packaged

- Examples of cost –
 - PHENIX EmCal - \$40/chan. (chips, boards, readout)
 - W/O ASICs, it would have been >\$100/chan.
 - ASICs may let you get down to \$10/chan. or less.

- The front-end pitch can also be made to complement the detector



The Great Question...

Is CMOS popular because it has outstanding analog performance, low noise, and extreme speed?

NO!

Because almost none of that is true....

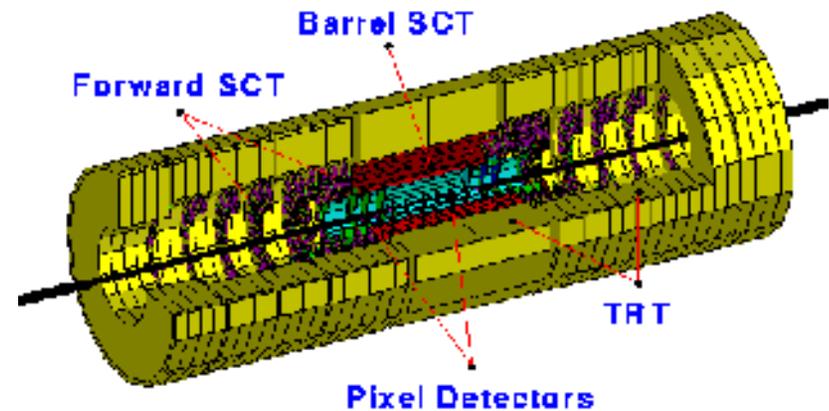
It's because you can make bazillions of Timex watches and Pentium processors cheaply and that's what drives the market.

(1 bazillion = $10^{\text{Intel stock price}}$)

ATLAS Pixel Detector

The ATLAS Pixel Detector

- Three barrel layers
- Consists of 2 m² of sensitive area
- This translates to 80 M readout channels
- Pixel size is 50 μm X 400 μm (Some are 50 μm X 300 μm)
- Radiation doses 10¹⁵-1 MeV n_{eq}/cm² with total dose of 50 Mrad



The disks

- Disks made of sectors
- Cooling provided by a glassy carbon tube between 2 Carbon-Carbon facings



The ATLAS Pixel Detector - Semiconductor Radiation Detectors in Particle Physics and Biomedical Imaging - Bad Honnef 19-21 June 2000

*Francesco Ragusa
MILANO*

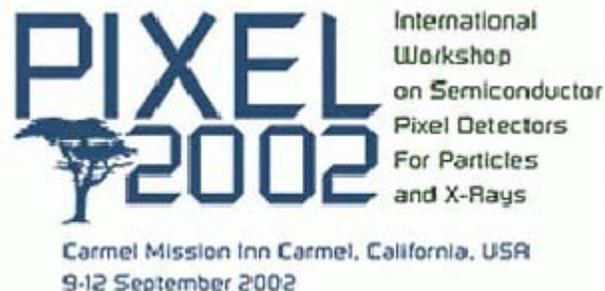


The Readout Architecture of the ATLAS Pixel System

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Copy of This Talk:

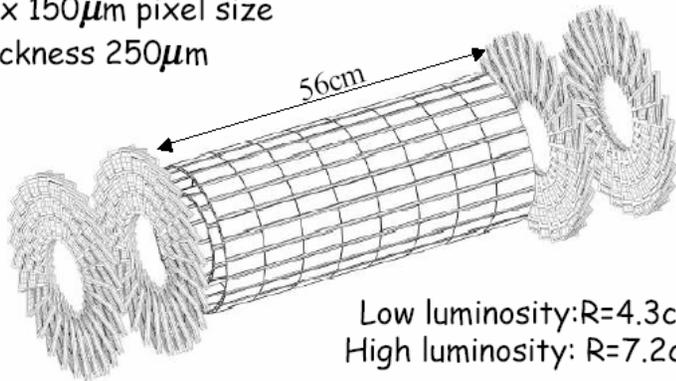
<http://www.ge.infn.it/ATLAS/Electronics/home.html>



CMS Pixel Detector

The Pixel Detector

100 μm x 150 μm pixel size
thickness 250 μm



Low luminosity: R=4.3cm and 7.2cm
High luminosity: R=7.2cm and 11.0cm

- The whole pixel system consists of about 50 millions pixels
- Single pixel counting rate will be about 10kHz
- Estimated resolution is about 15 μm

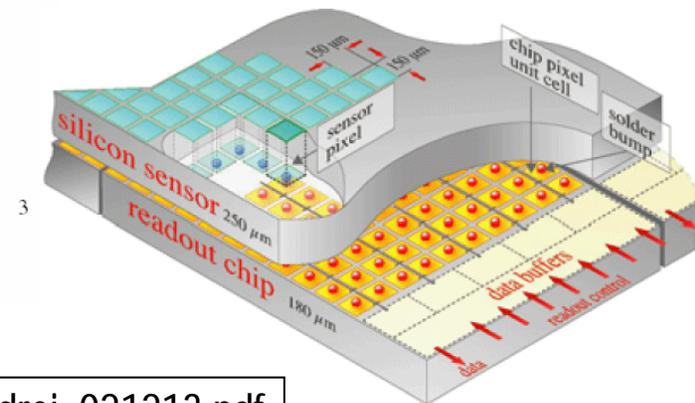
A. Dorokhov

Tests of Silicon Sensors for the CMS Pixel Detector

Andrei Dorokhov

University of Zurich

Friday, 13 December, 2002



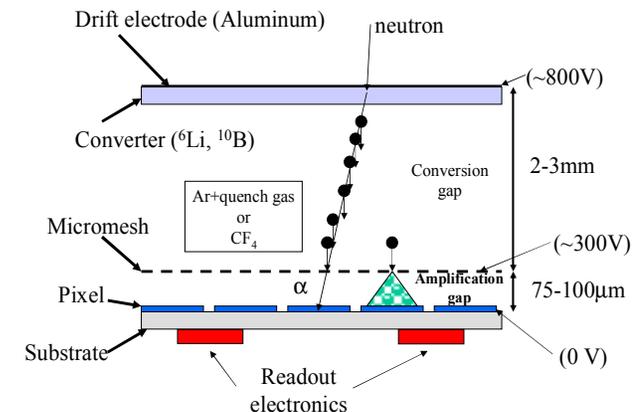
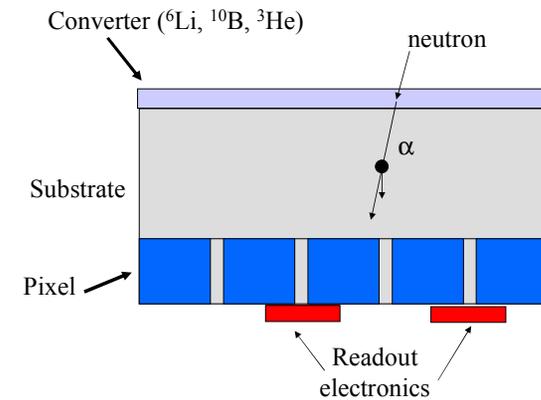
http://unizh.web.cern.ch/unizh/doc/zuerich/meeting_talks/andrei_021213.pdf

Other Pixel Detectors

Presently In Development at ORNL

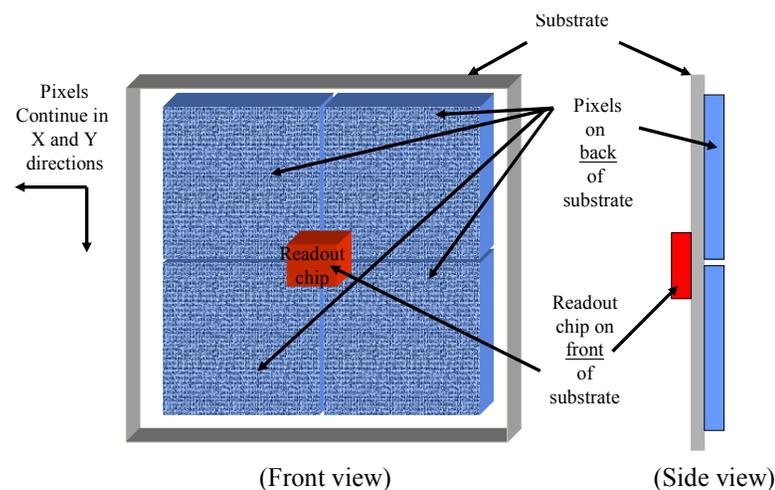
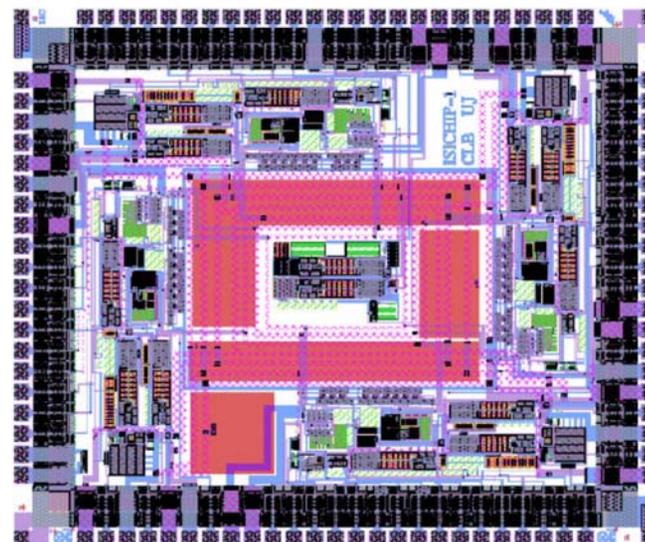
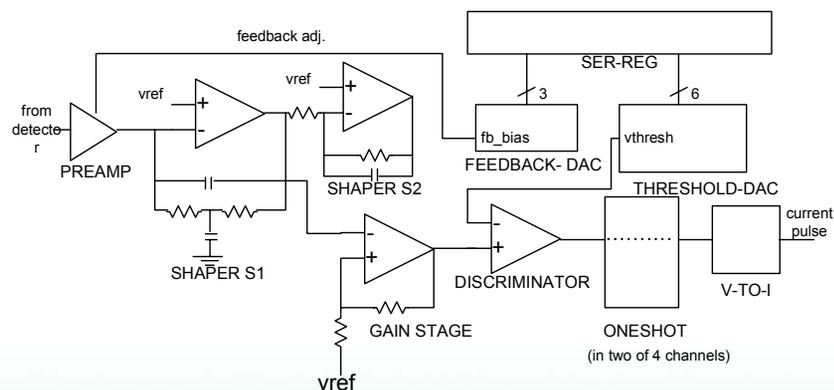
Two Different Pixel Detectors with Similar Readout Requirements (Pixel sizes $\sim\text{mm}^2$)

- The Solid-State neutron detector being developed by IntraSpec, Inc. of Oak Ridge utilizes converters (solid or He).
- Pixellated readout is accomplished by custom ASICs.
- The MicroMegas detector has recently been developed at CERN for high-energy, charged-particle detection.
- It is a pixellated gas-multiplying structure.
- We are developing it into a neutron detector we call the NeutroMegas.



The ISI chip was designed for the ISI neutron pixel array

- Process is 0.5 μ m AMI bulk CMOS process
- Process chosen for 5V V_{DD}
- Layout format is for quad corner mount
- Communications include –
 - Serial programming / non-destructive read-back (enables daisy chaining)
 - Current-mode outputs for low swing (quasi-differential)



Quad-pixel corner-mount electronics configuration

It should be clear now that pixel detectors don't offer any free lunches regarding the data plant

- Per-pixel occupancy vs. channel occupancy (*Law of Conservation of Difficulty*)
 - A true n^2 array ($n \times n$) reduces per-pixel rates by n^2 at the expense of a complex data communications plant
 - A $2n$ array reduces data plant by $2 \div n$ compared to n^2 array but only reduces per-channel occupancy by the same
- Pile-up effects must be considered for the entire channel
- In other words, no free lunch whether you're talking about a 2-D crossed-fiber array or a Zheng Li-type interpolating gas or solid-state detector (Stripixel)

So Detector Electronics Challenges Abound...

- We have lots of closely-coupled, on-detector electronics
- We need low scatter materials and configurations
- We have very high count rate in a few channels and lots of sparse channels but every channel must be able to handle max rate
- We therefore need to investigate smart, zero suppression front-ends
- All this will result in complex routing of readout architectures
- Very important – built-in test capability for detector channel reliability
- We still need to test the neutron hardness of some candidate semiconductor processes and the effects of assembly materials on gas purity
- **Some advice – Don't assume someone else's chip designed for some entirely different experiment will drop right in. Application Specific usually means just that. *None of the labs make catalog products.***

You need to read this....

An excellent paper for summarizing CMOS design for pixels - P. Fischer, "Design considerations for pixel readout chips", NIM A 501 (2003) 175-182.