

A Comparison between LBNL and LANL LLRF Control Systems

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A backup LLRF control system for the RFQ is currently under development at LBNL. It is based upon the existing MEBT rebuncher system, but with some changes and enhancements. The purpose of this note is to help in evaluating the viability of this backup system for the application of the RFQ and possibly beyond. Listed in the table below is a comparison between the two systems. The table only includes the basic methods and hardware features which I think really matter for the functionality of cavity field control. The LBNL system is assumed in basically its existing form for MEBT. While the LANL system is assumed to be in the form as described in its design document of current release. Some explanations are also included mainly for LBNL system. As you will see, the two systems are basically similar with an exception that LBNL design has implemented a method for solving the phase drift problem. Another thing that needs to be kept in mind is the LANL system is still in the stage of prototyping. There will inevitably be some change of plans during the development process. In the end, the system may be different from what is described here. For detailed information on the LANL system, please refer to the LANL system description document, LA-UR 01-0674, which is available on the LLRF Reviewer Materials web site at <http://www.sns.gov/projectinfo/llrf/>.

The comparison does not include anything related to EPICS and IOC.

Hardware & methods	LANL System	LBNL System
RF/IF/ADC Clock	402.5/50/40MHz	402.5/50/40MHz
IF channel bandwidth control	Fixed Analog IF + digital FIR filter	Fixed analog IF filter
General method of Phase/amplitude measurement of cavity field, waveguide forward, and reflected signal	Digital; 40MHz Quadrature sampling on the 50MHz IF of three input channels	Digital; 40MHz Quadrature sampling on the 50MHz IF of three input channels
Method for long-term stability of cavity phase measurement.	No. There is no correction for the clock phase drift. ¹	Yes. Differential phase measurement between the cavity and reference IF signal. ²
Sampling of IF signals	40MHz, 14-bit	40MHz, 12-bit ³
Phase/amplitude control of Klystron RF drive	Analog; Analog I/Q modulation on IF output. ⁴	Analog; Analog I/Q modulation on IF output.
Electronic LO stretcher	No	Yes ⁵
I/Q modulation DAC	16-bit	12-bit
Field Phase/amplitude feedback control method	Digital PID ⁶ , implemented in FPGA	Digital PID, implemented in FPGA

“Feed forward” pattern playback method	Digital in FPGA, FFWD pattern data is added into the data of control output outside the PID loop.	Digital in FPGA FFWD pattern data is blended into the feedback error data inside the PID loop, before the integrator.
FFWD waveform data calculation	in on board DSP	in IOC ⁷
FFWD data buffer	2x32kx32 FIFO ⁸	2x256x8 table ⁹
Cavity RF field data buffer	32kx32 ¹⁰	1024x10 ¹¹
Forward RF data buffer	32kx32	1024x11 ¹²
Reflected RF data buffer	32kx32	1024x11+1024x12 ¹³
Cavity resonance frequency detection	On-board DSP calculates the frequency error from the forward and reflected RF data, and passes the result onto EPICS ¹⁴	IOC calculates the frequency error from the Hi-Resolution reflected RF data, and passes the result onto EPICS
RF drive frequency variation for “cold-start”	Switching to a separate DDS ¹⁵	Frequency shift of IF drive through vector rotation controlled by FPGA. ¹⁶
High-power protection	Analog RF power monitors in HPM for “forward”, “reflected” and “cavity field” + arc detector I/O in HPM ¹⁷	Analog RF power monitors in RF chassis for “forward”, “reflected” and “cavity field” + digital RF power monitors in FPGA. There is a single MPS interlock port, but no separate arc detector input ports.
Misc. ADC channels for system monitoring	8+, multiplexed ¹⁸	8, multiplexed
Ultimate action in an event of fault	Kill RF drive to Klystron + informing MPS	Kill RF drive to Klystron + informing MPS

¹ LANL design only performs a “single-ended measurement” on cavity phase with a reference to the absolute phase of the 40MHz ADC clock. When the phase of the clock drifts, and so does the measurement result. In this case, the error with the phase reference which the FRCM actually gets is the error of the original reference plus the error of the clock generator (CDM).

² LBNL design performs a “differential” phase measurement on both the cavity field and the reference signal with the same ADC clock. Therefore, the error caused by the clock phase drift gets cancelled. The digital board directly uses the original reference for determining the cavity phase, eliminating the contribution from the clock error. The cavity and reference are sent to the digital board through two separate channels for phase measurement. To keep ADCs cool, the power for ADCs is only turned on for about a

millisecond per pulse. An extended acquisition for 50 uS or so both before and after the main pulse is made to collect the reference signal. A control signal for multiplexer is also planned. That will allow the experimentation of sending the cavity field and reference signal through a single channel in different time, thus to eliminate the error of channel mismatch, beside the clock drift.

³ To put it in perspective, a 12-bit ADC translates into a maximum amplitude and phase measurement resolution of $\pm 0.1\%$ and ± 0.03 degree, assuming 11 effective bits out of the 12.

⁴ If the I/Q modulation is done digitally, the range of the phase shift will be unlimited. With a non-linear analog modulator, however, the phase shift will have to be limited within a certain range to avoid the excessive signal compression in certain operating regions.

⁵ Because of the compression regions with an analog I/Q modulator as mentioned above, the I/Q modulator needs to work around a certain operating point. But when the operating condition of the Klystron changes, the phase will change significantly, and I/Q modulator will be forced away from the desired region. To move the phase of the modulator back to the desired operating point, the LO phase offset needs to be adjusted to compensate the Klystron phase change. The “LO” stretcher does just that.

⁶ PID stands for “Proportional-Integral-Differential”, a classic closed-loop control method. In LBNL system, the “D” is not implemented (equivalent to setting the differential gain to zero) as it is not needed. Likely that will also be the case in LANL system.

⁷ The IOC is “nanoEngine” from Bright Star Engineering. Despite of its tiny size, NanoEngine is a powerful 32-bit RISC processor, packed with 32Mb memory, and Ethernet ready. It runs at a speed of 200MIPS (200 million instructions per second, not every computer issues one instruction per clock cycle – a Pentium II averages about two, older 68k machines usually rate about one half). The computation power of the nanoEngine is enough to run the six-degree-of-freedom pseudo-nonlinear curve fit of the reflected signal waveform in under 1 millisecond.

⁸ The 32k complex (real & imaginary) FFWD data is directly played back as it is in a speed of 20MHz. The 2x32k data block will last for about 1.6ms. The 32Kx32 history buffers are currently implemented with the external FIFO memories on the Rev. A and C FRCM board. As I understand it, there is a possibility that in future revision, the external memories will be eliminated, and the history buffers will be implemented with the FPGA internal RAM, and the buffer size will be reduced to to 1kx32.

⁹ $2 \times 256 \times 8 \rightarrow$ feed forward waveform data: The Feedforward table holds 512 x 8 entries, which are interleaved I and Q. Thus there are only 256 complex entries. Different from LANL design, the FFWD data in LBL system is added into the feedback loop before the integrator. Because of that, the FFWD data buffer in LBNL system only stores the

increment/decrement data (like a “delta M” coding scheme). Therefore, the 8-bit represents the resolution of the data increment, not the resolution of entire signal amplitude. The resolution of the FFWD waveform is full 12-bits of the DAC, although the encoding scheme limits the slew rate, such that a full scale change takes at least 1.6 us (but remember the time constant of the DTL cavity is more than 10 times of that). The complex FFWD data is played back at a rate of 200ns per complex data point.. However, because the FFWD data is added into the DSP process before the integrator, its effect lasts forever. A note from Larry: The possibility of inter-pulse feedback is supported by the hardware (at least for the first 50 microseconds of the pulse), but has not been tested at this point. All the runs to date have used a fixed (operator adjustable) feedforward table.

¹⁰ The 32k complex (real & imaginary) FFWD data is directly played back as it is in a speed of 20MHz . The 2x32k data block will last for about 1.6ms. The 32Kx32 history buffers are currently implemented with the external FIFO memories on the Rev. A and C FRCM board. Again, the buffer size might be reduced to to 1kx32 in future revision.

¹¹ 1024x10 → cavity field data buffer: for the field regulation, the cavity field data buffer is not needed at all. To record a history trace of 1ms or longer, the original data of 20MHz sampling rate will needs to be decimated. Due to the fact that the DTL cavity bandwidth is only 23kHz, the raw data can be decimated by a factor of 100 (equivalent to a 100kHz sampling rate) without losing any information. The 10-bit resolution of the raw data can be improved by data averaging before decimation.

¹² 1024x11 → forward power data buffer: same as the cavity field data, this buffer records the history trace of the forward wave in the waveguide. Similarly, the technique of decimation for data compression can also be used here for recording an 1ms or longer signal trace.

¹³ 1024x12 → reflected wave: higher resolution data buffer for a closer look at the rise edge of reflected wave. The data in this buffer is used for calculating the cavity resonant frequency. If sampled at the full speed of 10MHz for 4-data group (I.Q.-I-Q), the record length will be 25 us, containing 512 phase/amplitude measurements.

1024x11 → reflected power: this lower resolution data buffer records the history trace of the reflected power over the entire 1 ms pulse width. The data decimation is also needed. All table sizes are adjustable in firmware, subject to the limit of total available 12 blocks of 4096 bits each.

¹⁴ According to LANL design document, the plan was to carry out the task of resonance frequency calculations with the IOC. But currently, it is done with the on-board DSP.

¹⁵ The current version has a dedicated DDS on the RF board to generate the off-50MHz output. A synchronous clock has been planned for the future revision.

¹⁶ In drive frequency shift mode, the FPGA generates a Sine and Cosine control signal to rotate the 50MHz IF drive vector through the I/Q modulator at an angular speed of $2\pi\Delta f$. Thus the frequency of IF out is shifted by Δf .

¹⁷ LANL HPM has history buffers to store the analog RF power detector output traces digitized at a rate of 1MHz by an 3-1/2 digit ADC.

¹⁸ Complete information is unavailable.