



High-Power-Protect Module

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5 High-Power-Protect Module

The High-Power-Protect Module (HPM) detects faults in the High-Power Distribution System and interfaces the radio-frequency control system (RFCS) with the Machine-Protection System (MPS) and the RF_PERMIT_HARD input from the vacuum system. For the fault-detection function, it monitors the High-Power RF Distribution System for over-threshold conditions, detects cavity-arc faults, and responds to arcs in the Waveguide-Distribution System. Arcs in the Waveguide-Distribution System are detected by an Advanced Ferrite Technologies (AFT) fiber-optic arc-detection chassis in the HPRF rack. The chassis sends a fault signal called an FOARC to the HPM.

For the system-interface function, the HPM receives the hardware signal (RF_PERMIT_HARD) from the Vacuum Programmable Logic Controller (PLC) System. This enables the RF carrier, but does not turn it on. In the event of a fault, the HPM asserts (pulls low) the MPS_PERMIT signal to the MPS, signaling the MPS to abort the beam and shut off the pulse. The various setpoints and reporting functions are accessible through the Experimental Physics and Industrial Control System (EPICS). There is also an EPICS-accessible software RF_PERMIT_SOFT function.

5.1 HPM Architecture

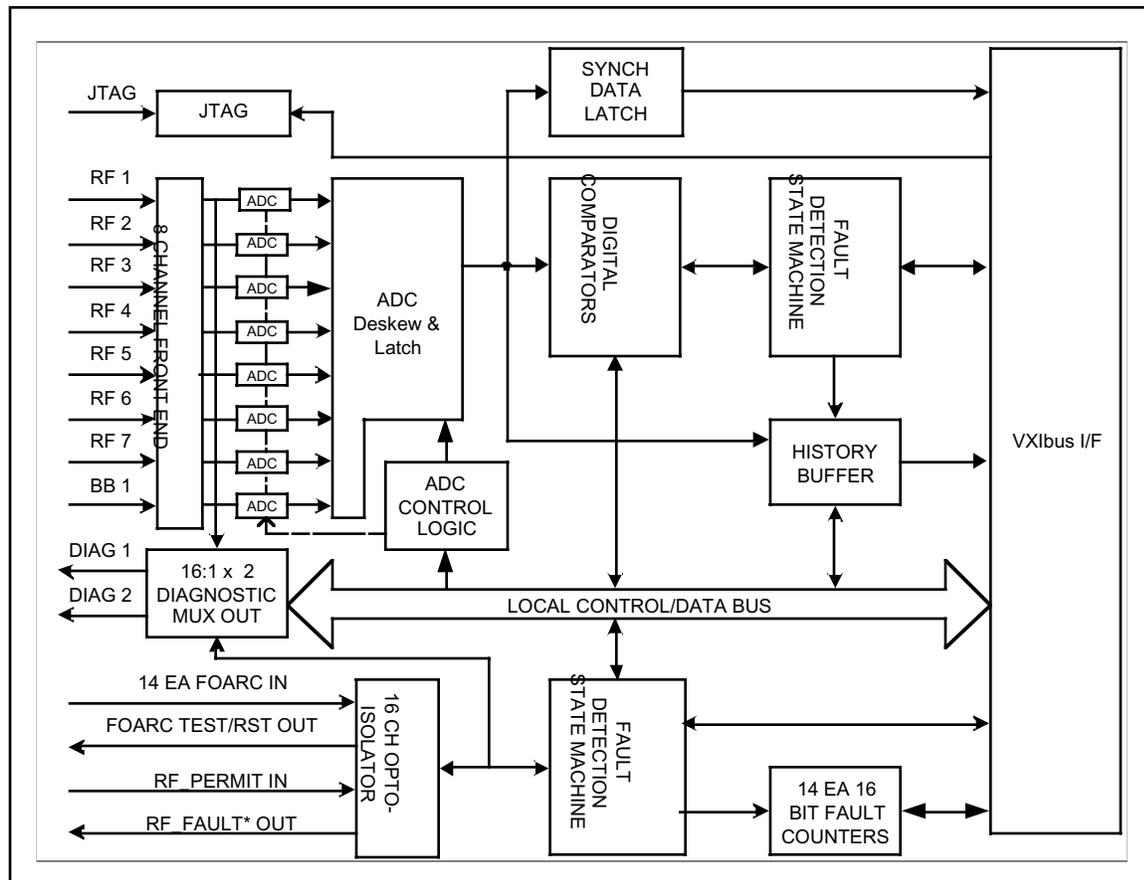
Figure 5-1 shows a simplified block diagram of the HPM. Each HPM may monitor up to seven RF channels (RF 1–7) and fourteen FOARC channels, complying with the requirements. The functions of the RF channels and the FOARC channels will be considered separately. In broad terms, the RF inputs are conditioned and then digitized. The first seven are assigned to RF control and monitoring functions while channel 8 of the analog-to-digital converter (ADC) is not used at this time. The data from all the analog channels may be latched on command from EPICS to provide a synchronous sample throughout the system and may be directed to the front panel test points through the two diagnostic multiplexers.

There are three major logic blocks in the HPM (see Figure 5-1). The first block (right side) is the VXIbus interface (I/F) circuit designed by Matt Stettler of the Global Controls Group (SNS-4) at LANL. This proven design serves as the interface between the logic of the HPM and the VXIbus backplane. The backplane in turn communicates with the input/output controller (IOC). The second block is the RF channel fault-detection-state machine. This block manages the ADC, latches, comparators, and RF fault-detection logic. The third major logic block comprises the FOARC counters and their fault-detection logic. All of the logic works on clocks derived from the 40-MHz clock off the backplane. A built-in 40-MHz clock is available in the HPM for debugging purposes, but the backplane clock should be used for normal operation.

Event counters and timers are 16-bits wide and are based on a 1-MHz clock, for a maximum timer duration of 65.5 ms. All of the logic is accommodated in a single Altera

programmable logic device (PLD), programmed via a Joint Test Action Group (JTAG) connector on the board, or via the VXIbus interface to the backplane.

Figure 5-1. HPM Top-Level Block Diagram



5.2 HPM RF Fault Management

The HPM monitors the various RF inputs and, based on whether they are above or below a threshold, takes actions to protect the system. The two fault-maturation strategies, used to improve noise immunity and to avoid nuisance trips, are fill time and persistence.

The fill-time strategy is not to look when transients are being generated during normal operations. When the RF carrier is gated on (via TTLTRG3*), the HPM ignores faults on all the RF channels (but not the FOARC channels) for the duration of FILL_TIME. For normal-conducting (NC) cavities, we anticipate that the FILL_TIME will correspond to the actual fill time of the cavities. For superconducting RF (SRF) cavities, we expect that FILL_TIME will actually be shorter than the SRF cavity fill time (which is about



100 μs –200 μs), and will be just long enough to allow a reasonable amount of cavity field to build before enabling the RF fault-tripping algorithms.

The persistence strategy is to use a duration timer (RF_DLY_HI). The timer sets a minimum period for which a fault must persist before it is matured as a fault event, thus discriminating against short transients. Both of these functions may be disabled by setting their durations to zero.

5.2.1 Cavity Arc Detection

The HPM monitors two kinds of RF faults, excessive RF power at the various RF waveguide test points, and arcs internal to the accelerator cavity. Detection of excessive RF power is straightforward because it is a simple time-over-threshold function. Detection of a cavity arc is more difficult. The LANL Low-Energy Demonstration Accelerator (LEDA) radio-frequency quadrupole (RFQ) arc-detection strategy could not distinguish between a cavity arc and the cavity moving off-resonance because both caused high reflected power. If the cavity has arced, the system must shut off the RF until the arc clears; if the cavity is off-resonance, the system must continue to deliver RF power to pull it back to the operating frequency.

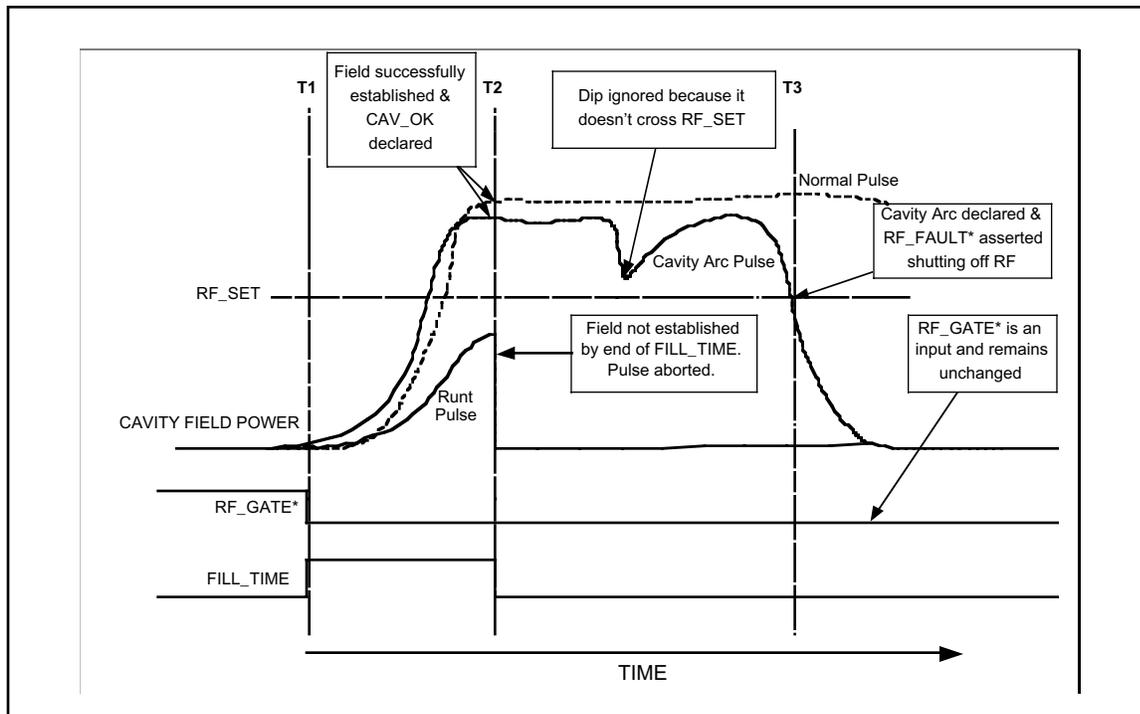
The HPM implements the cavity-arc-detection strategy suggested by Lloyd M. Young of SNS Division Office at LANL for both NC and SRF cavities (see Figure 5-2). This strategy monitors the RF power level in the cavity and correlates that against the RF_GATE* (TTLTRG3*) and FILL_TIME. FILL_TIME is triggered by RF_GATE* and starts coincidentally with it.

There are three possible operational scenarios for cavity field faults. In the first (Normal Pulse), the cavity field power rises above the threshold set by RF_SET before FILL_TIME expires. As long as it remains above RF_SET for the duration of the macropulse, all is well.

In the second scenario (Cavity Arc Pulse), the field is successfully established as in a Normal Pulse, then the cavity arcs, shorting out the field. Small dips in the cavity field are ignored, but once the cavity field drops below RF_SET, the arc is declared and the pulse is aborted at T3.

The third scenario (Runt Pulse) is when the field fails to reach RF_SET before FILL_TIME expires. When this happens, the pulse is immediately aborted at the end of FILL_TIME (T2). The times in Figure 5-2 are not to scale.

Figure 5-2. Cavity Arc-Detection Logic



5.2.2 RF Fault Actions

Once a fault has been matured and declared, the HPM blanks the RF carrier until the end of the macropulse by asserting TTLTRG5* (RF_PERMIT_L), TTLTRG2* (RF_PERMIT_C), or TTLTRG7* (RF_PERMIT_R) on the backplane (selected by switches on the module), and notifies the MPS via the MPS_PERMIT output. If the fault persists through the interpulse period, the fault lines are held low until it clears. Examples of possible long persistent faults are a power-supply failure or a Clock Distribution Module (CDM) phase-locked loop fault.

5.2.3 Chatter Faults

Occasionally a klystron will fault repeatedly on every pulse attempt. These faults must be detected and the machine latched off until an operator identifies the source of the problem and restarts the machine. This chatter-fault-detection and latching function is built into the local IOC (in the same crate as the RFCS) such that the EPICS network is not required to protect the machine. The precise algorithm is **TBD**.



5.3 HPM RF Channel Inputs

Each HPM card has seven identical RF-processing channels consisting of a fixed attenuator, a broadband termination, and an Analog Devices AD8313 detector log-video amplifier. The output of the AD8313 is followed by a pair of wideband video buffer amplifiers used to adjust Zero and Span. There is also a provision for a baseband input channel (the unused channel 8). Each channel is digitized by a 10-bit ADC (AD7470), and all ADCs receive a simultaneous convert command, eliminating data skew between channels. A state machine in the Altera PLD controls the digitizing process and data management, with each channel updated every 2 μ s. A channel mask (settable via EPICS) is available to ignore unused channels. The ADC sample latency (from the time a sample is taken to the time it appears on the digital bus) is **TBD**.

Notice that there are no frequency-selective components in the RF-input-channel processing chain because the RF Accelerator Technology Group (LANSCE-5) will provide bandpass filters on their inputs to the HPM channels.

Table 5-1 summarizes the general RF characteristics for HPM channels 1-7.

Table 5-1. General Characteristics for All HPM RF Channels

Parameter	Value
RF input power level for specified operation	+10 to -40 dBm Withstand power level (no damage) +20 dBm minimum
Input return loss ($F_0 \pm 5$ MHz)	12 dB minimum (re: 50 Ohms)
Operating frequency	402.5 MHz or 805 MHz, depending on the application
Power-detection method	Detector log-video amplifier (AD8313)
ADC resolution	10 bits
RF connector type	8-channel blind-mate PKZ

5.3.1 RF Channel Power Measurement

The HPM uses an AD8313 detector log-video amplifier, which means that the output of the detector is equal to the logarithm of the detected signal amplitude. With appropriate scaling, this measures the RF power of the signal in dBm. The HPM detection circuits are calibrated to output $+2.450 \pm 0.005$ V with an input of +10 dBm at the front panel, and $+0.450 \pm 0.005$ V with an input of -40 dBm. This scales the output of the detector to 50 dBm/2.00 V or 25 dBm/V. The dynamic range of the detector at the -1 dB uncertainty level is on the order of 60 dB (+10 dBm to -50 dBm). There are no explicit frequency-selective components in the RF detector chain; the purpose of calibrating the HPM as a -G01 (402.5 MHz) or a -G02 (805 MHz) is to compensate for differences in the detector response at the two frequencies.



Given a 10-bit (1023 count), 2.50 V ADC, resolution is 2.44 mV or 0.06 dBm. ADC accuracy is specified at ± 2 counts, worst case, or ± 0.1 dBm. If the operator would like the displays to be in watts rather than dBm, EPICS must perform the conversion.

5.3.2 RF Channel Assignments

The RF input connector is an 8-channel blind-mate PKZ made by The Phoenix Company of Chicago, P/N P88P16DDF, with RF channels 0–6 corresponding to connector inputs 1–7, in numerical order. Table 5-2 shows the RF channel assignments for each stage of the accelerator.

Table 5-2. HPM RF Channel Assignments

RF Channel and PKZ Input Number	RFQ	DTL	CCL	SRF	HEBT
1	CAV_FLD_RF	CAV_FLD_RF	CAV_FLD_RF	CAV_FLD_RF	CAV_FLD_RF
2	CAV_FWD_RF	CAV_FWD_RF	CAV_FWD_RF	CAV_FWD_RF	CAV_FWD_RF
3	CAV_RFL_RF	CAV_RFL_RF	CAV_RFL_RF	CAV_RFL_RF	CAV_RFL_RF
4	CIRC_LD_RFL	CIRC_LD_RFL	CIRC_LD_RFL	CIRC_LD_RFL	CIRC_LD_RFL
5	MUX1_RF	CAV_PU	CAV_RFL_RF_2	KLY_FWD_RF	CAV_PU
6	MUX2_RF	NC	SPL_LD_RFL	KLY_RFL_RF	NC
7	NC	NC	CAV_PU	NC	NC
8 (NC)	N/A	N/A	N/A	N/A	N/A

5.4 HPM Fiber-Optic Arc-Detector Inputs

The HPM has fourteen FOARC inputs that are optoisolated at the HPM to avoid impulse noise and ground-loop problems caused by long cable runs between the HPM and the klystron controllers. The lower ten optoisolator inputs (channels 0–9) are all returned to a common ground in the HPRF rack, which is isolated from the HPM VXIbus crate ground. The grounds for the upper four channels may be strapped to the common (remote) ground, via jumpers on the board, or they may be returned to a ground elsewhere in the system, adding flexibility for on/off inputs to the HPM in the future.

When an FOARC is detected (HPM input goes low), the HPM turns off the RF carrier (dropping RF_PERMIT_L, RF_PERMIT_C, or RF_PERMIT_R on the backplane) and drops MPS_PERMIT to the MPS until the end of the macropulse or until the fault clears, whichever is longer. A channel mask (set via EPICS) is provided to ignore unused FOARC channels.



The FOARC_HIST[ory] function is implemented as a 16-bit counter on each FOARC channel. Each time an FOARC is detected, its corresponding counter is incremented. These counters continue to count until EPICS resets them. They may be used to generate histograms for off-line analysis. These counters are read and cleared individually via EPICS and are volatile (lost on power-down of the module). A flag is sent to EPICS when bit 15 of the counter is set, requesting a read/reset of the counters prior to overflow.

The FOARC function includes a built-in-test (BIT) function (also optoisolated) that may be activated via EPICS. The FOARC_TST signal to the AFT fiber-optic arc-detection chassis faults all the FOARC channels. On release, EPICS asserts an FOARC_RST to the AFT chassis, restoring normal operation.

The FOARC response time (the time between the input line going low and MPS_PERMIT going low) is TBD. The FOARC input connector is an AMP 747842-5, 25-pin male right-angle D-subminiature connector. Table 5-3 shows the connector-pin assignments at the HPM.

Table 5-3. HPM FOARC Connector-Pin Assignments

Pin Number	Function	Pin Number	Function
1	FOARC 00 High side	15	NC
2	FOARC 01 High side	16	NC
3	FOARC 02 High side	17	+5V_REM
4	FOARC 03 High side	18	NC (GLOBAL_ARC)
5	FOARC 04 High side	19	FOARC_RST (Part of self-test)
6	FOARC 05 High side	20	FOARC_TST (Part of self-test)
7	FOARC 06 High side	21	GND_REM_1 (Primary Ground)
8	FOARC 07 High side	22	GND_REM_10 (Auxiliary Ground for FOARC 10)
9	FOARC 08 High side	23	GND_REM_11 (Auxiliary Ground for FOARC 11)
10	FOARC 09 High side	24	GND_REM_12 (Auxiliary Ground for FOARC 12)
11	FOARC 10 High side	25	GND_REM_13 (Auxiliary Ground for FOARC 13)
12	FOARC 11 High side		
13	FOARC 12 High side		
14	FOARC 13 High side		



5.5 HPM Fast Machine-Control Interfaces

The high-speed interface between the RFCS and the Machine-Control System is through a pair of optoisolated digital channels in the HPM. The vacuum PLC provides the HPM with an RF_PERMIT_HARD signal that enables the RF carrier, but does not turn it on.

The HPM notifies the MPS of any faults in the local RFCS via an optoisolated MPS_PERMIT output. The interface to these two external systems at the HPM end is a Weidmuller P/N 1728630000 6-pin receptacle that mates with a Weidmuller P/N 174817000 plug. Table 5-4 shows the pin assignments for this interface at the HPM.

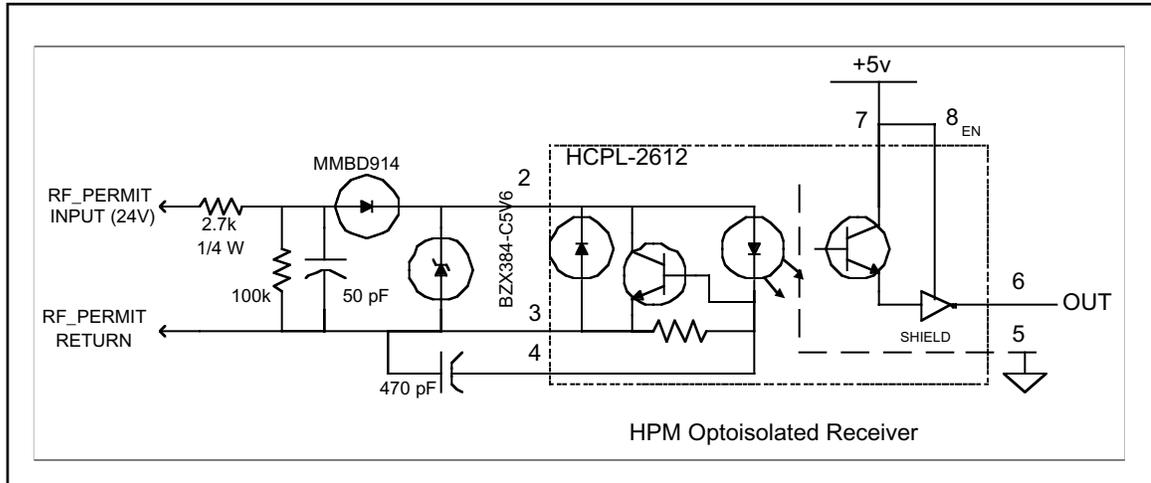
Table 5-4. HPM Interface Connector-Pin Assignments

Pin Number	Function
1	MPS_PERMIT output high side (current-limited +5V to MPS optoisolator input)
2	MPS_PERMIT output low side (return for MPS optoisolator input)
3	Loop-back input from MPS
4	Loop-back output to MPS
5	RF_PERMIT_HARD input high side (current-limited +24 V to HPM optoisolator input)
6	RF_PERMIT_HARD input low side (return for HPM optoisolator input)

5.5.1 RF_PERMIT_HARD Input

The HPM provides an optoisolated input for the RF_PERMIT_HARD signal from the vacuum PLC, as shown in Figure 5-3. The logic is such that a high (current into the HPM) = OK, and a low (no current into the HPM) = Fault. In the event of an RF_PERMIT_HARD fault, the MPS_PERMIT output will be asserted for the duration of the fault. The response time (the time between the RF_PERMIT_HARD input line going low and the MPS_PERMIT output going low) is **TBD**.

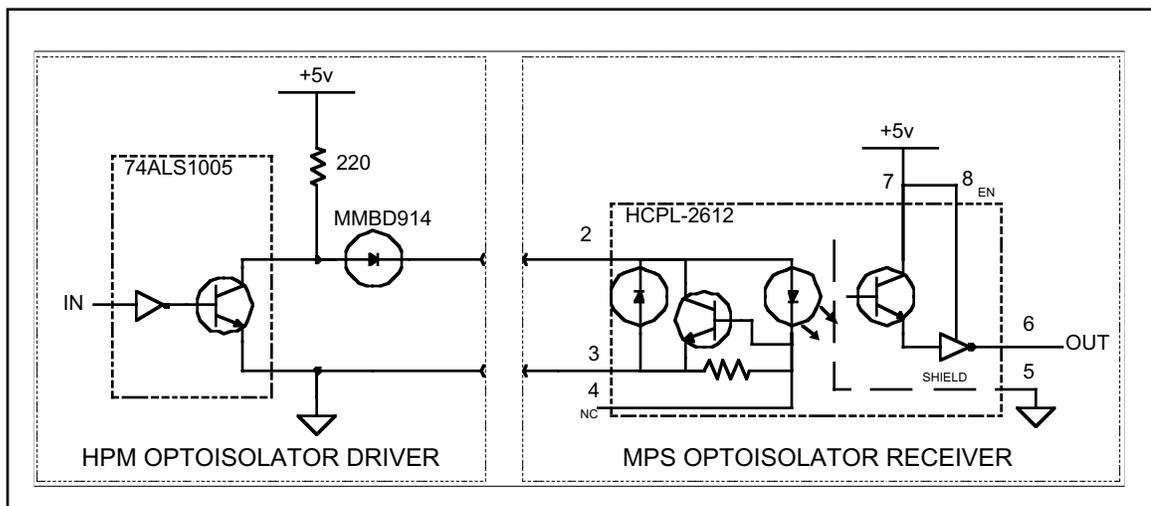
Figure 5-3. RF_PERMIT_HARD Input



5.5.2 MPS_PERMIT Output

The HPM provides an open-collector output to drive an MPS interface module, per Figure 5-4. The logic is such that a high (current out of the HPM) = OK and a low (no current out of the HPM) = Fault. Note that the HPM does not read (monitor) the MPS_PERMIT signal, it can only assert it. The response time (the time between RF_PERMIT_L/C/R going low and the MPS_PERMIT going low) is **TBD**.

Figure 5-4. MPS_PERMIT Output to MPS





5.6 HPM Diagnostic Multiplexer

There are a pair of single-pin LEMO 50-Ω connectors on the front panel that allow monitoring of the various analog, FOARC, and TTLTRG* channels selected by a pair of analog multiplexers (A and B) on the board. The multiplexers are addressed via EPICS. The A_GND/SPARE channels are configured such that a jumper wire from anywhere on the board can be assigned to the multiplexer inputs for debugging purposes. Table 5-5 describes the diagnostic multiplexer addressing scheme.

Table 5-5. Diagnostic Multiplexer (MUX) Channels

EPICS Channel Number	Mux A Function	Mux B Function
00	A_GND/SPARE	A_GND/SPARE
01	TTLTRG0*	ADC_IN0 (RF Channel 1)
02	TTLTRG1*	ADC_IN1 (RF Channel 2)
03	TTLTRG2*	ADC_IN2 (RF Channel 3)
04	TTLTRG3*	ADC_IN3 (RF Channel 4)
05	TTLTRG4*	ADC_IN4 (RF Channel 5)
06	TTLTRG5*	ADC_IN5 (RF Channel 6)
07	TTLTRG6*	ADC_IN6 (RF Channel 7)
08	TTLTRG7*	ADC_IN7 (ADC Channel 8))
09	FOARC_00	FOARC_07
10	FOARC_01	FOARC_08
11	FOARC_02	FOARC_09
12	FOARC_03	FOARC_10
13	FOARC_04	FOARC_11
14	FOARC_05	FOARC_12
15	FOARC_06	FOARC_13

5.7 HPM History Buffer

The HPM has a 2-channel by 1024-location by 16-bit-word history buffer that can simultaneously monitor any two HPM channels selected via the HISTBUFF_SRC command in EPICS. The contents of the history buffer are always written at a 500-kHz rate, triggered by RF_GATE*, beginning at address location zero and proceeding until all 1024 locations for each buffer are filled. This gives a record length for each channel of 2048 μs, or enough to see any ring-down effects after the end of the macropulse.



DIAG_MUX_CTL bits 14 and 15 control the history-buffer refresh. If bit 15 is set, the next (global) SAMPLE* pulse freezes the history buffer at the completion of the 1024 samples and prevents it from being overwritten until bit 15 is cleared. This permits the capture of a “snapshot” of the channel history before and after the SAMPLE* event. If bit 14 is set, the history buffer is frozen at the completion of the next macropulse acquisition. If both bit 14 and bit 15 are set, the system defaults to the bit-14 condition, capturing one macropulse-worth of data and then freezing.

5.8 HPM Front-Panel Indicators (LEDs) Normal/Fault Colors

Table 5-6 shows the colors and meanings of the front-panel indicators.

Table 5-6. HPM Front-Panel Indicators

LED Signal	LED Color	Indication
MODSEL	Yellow	The HPM Module has been selected by the IOC (input).
	Black	The HPM Module has <i>not</i> been selected by the IOC.
RF_GATE	Green	RF_GATE* (TTLTRG3*) is low (i.e., RF-enabled).
	Black	RF_GATE* (TTLTRG3*) is <i>not</i> low (i.e., RF is not enabled).
FOARC_FLT	Green	The FOARC cable is connected and all inputs are high (OK).
	Red	The cable is disconnected or an FOARC command has been received from the AFT chassis (Short Blink).
RF_PERMIT	Green	RF_PERMIT_HARD input is high (OK).
	Red	RF_PERMIT_HARD input is low (Fault).
HPM_FLT	Green	The HPM is <i>not</i> declaring a fault.
	Red	The HPM is declaring a fault
MPS_PERMIT	This LED is triggered by any RFCS module in the crate. In conjunction with the other indicators, this LED allows the operator to troubleshoot the origin of a fault. For example, if MPS_PERMIT is red (faulted) but FOARC and HPM_FLT are green, it means that the HPM is OK; therefore either the CDM or the field/resonance control module (FRCM) has generated the fault via the backplane.	
	Green	The HPM MPS_PERMIT front panel output is high (OK).
	Red	The HPM MPS_PERMIT front panel output is low (Fault).



5.9 HPM Front and Rear Panel Signals

Front Panel Inputs	Signal Level	Frequency
FOARC Connector	Opto-TTL	100 μ s PW
RF_PERMIT_HARD	Opto-TTL	N/A
RF Channels 1-7	+10 dBm Max	402.5 MHz or 805 MHz per calibration

Front Panel Outputs	Signal Level	Frequency
MPS_PERMIT	Opto-TTL	N/A
DIAG_MUXA	Baseband Analog/TTL	<10 MHz
DIAG_MUXB	Baseband Analog/TTL	<10 MHz

Backplane Inputs	Functionality When Driven Low	Backplane
40 MHz	ADC Sampling Clock	ECLTRG0
SYNCH (10 MHz)	I/Q Synchronization Pulse	ECLTRG1
SAMPLE*	Save data to buffers	TTLTRG0*
SRF_TUNE*	Ignore RF faults for SRF_TIME	TTLTRG1*
RF_PERMIT_C	Shut off center RF carrier	TTLTRG2*
RF_GATE*	Carrier-enable input from timing	TTLTRG3*
PREPULSE*	RF pulse-timing fiducial	TTLTRG4*
RF_PERMIT_L	Shut off left RF carrier	TTLTRG5*
MPS_PERMIT	Shut off MPS_PERMIT	TTLTRG6*
RF_PERMIT_R	Shut off right RF carrier	TTLTRG7*

5.10 HPM Built-in Test and Calibration Functions

Because the primary purpose of the HPM is to protect the machine from HPRF faults, several measures have been included for built-in test (BIT) and accuracy enhancement. The HPM also has several technician-friendly features to simplify maintenance and troubleshooting. These are described below.

5.10.1 ADC Self-Test and Accuracy Enhancement

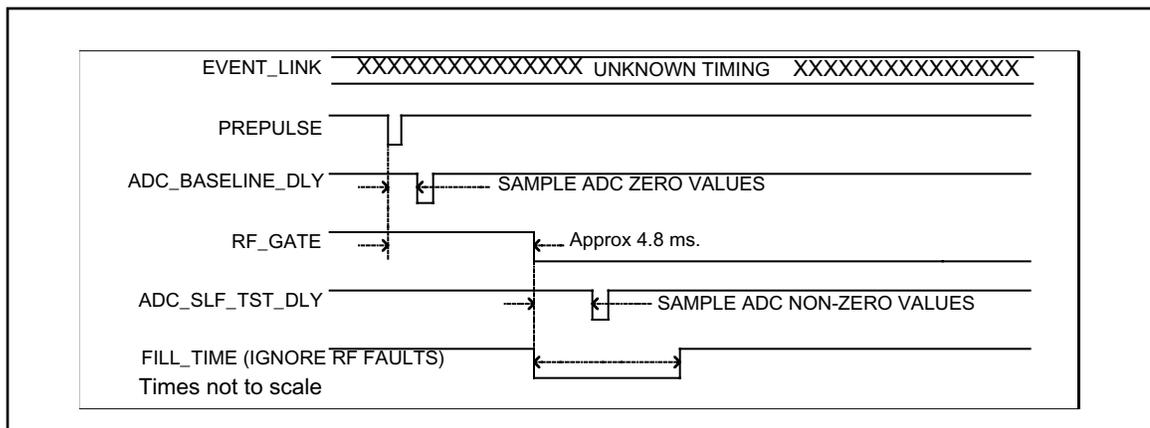
The function of the first BIT feature is to assure that the ADC channels are receiving inputs. A stuck-at-zero fault on an ADC channel or a disconnected RF cable could cause machine damage by not detecting a true RF fault.

Refer to Figure 5-5. On the falling edge of PREPULSE, the outputs of the ADC are latched after ADC_BASELINE_DLY for subtraction from the data values occurring later in the pulse. This is the zero-offset voltage of the ADC, which is measured when there is no RF present in the system. Sometime later (set by the EVENT_LINK parameters), the RF_GATE signal drops, enabling the RF carrier. The ADC_SLF_TST_DLY waits a few

microseconds for the RF to come up off zero and then samples the RF channels to compare them against ADC_SLF_TST_VAL.

This is a diagnostic that allows the HPM to detect an open line or a stuck-at-zero fault; it will not detect a stuck-high channel. ADC_SLF_TST_DLY should be approximately half of FILL_TIME so that the HPM has time to switch the comparator thresholds for the BIT ADC_SLF_TST_VAL to the RF fault threshold values prior to the end of FILL_TIME. Take care to avoid conflicts between this BIT function and the SAMPLE* function. Conflicts should not occur as long as SAMPLE* does not occur during FILL_TIME. Masked channels will be ignored. A stuck-high fault would shut off the RF, so this would cause no damage to the machine.

Figure 5-5. Pulse-Setup Timing



5.10.2 Power-Supply Monitoring

The second BIT monitors the power-supply voltages generated on-board (high = OK). VXIbus crate power supplies are assumed to be monitored elsewhere. In the event of a power-supply error, the module faults the MPS_PERMIT line to prevent improper operation.

5.10.3 Clock Monitoring

The third BIT detects failure of the 40-MHz CDM clock. A watchdog timer asserts a fault if the PLD does not reset it in time. For troubleshooting convenience, an on-board 40-MHz clock is provided and is selectable via a jumper. The position of the jumper is readable via EPICS to assure that, under normal operation, the HPM is using the clock provided by the CDM.



5.10.4 RF_FLT_TST

Asserting this EPICS function simulates an RF_PERMIT L/C/R in the HPM, triggering the MPS_PERMIT output to the MPS and lighting the LED for HPM_FLT.

5.10.5 FOARC_TST/ FOARC_RST

Asserting FOARC_TST via EPICS will command the HPRF FOARC circuitry to assert the “lamp test” function in the AFT transmitter in the HPRF rack, faulting all the FOARC channels in the HPM. EPICS follows it with an FOARC_RST command to restore the FOARC transmitter to the operational state.

5.10.6 On-Board Diagnostic Connector

The HPM provides five on-board diagnostic and control connectors for debugging the board. The pin assignments are shown in Table 5-6 below. These connectors are set up to accept 2 x 8 logic-analyzer probes directly. The bottom row of each connector is grounded.



Table 5-7. HPM Diagnostic Connector-Pin Assignments

VXI Address and Power Supplies—J1			
SAMTEC P/N ASP-32646-01			
Pin	Name	Pin	Name
1	GND	2	VXI_A1
3	GND	4	VXI_A2
5	GND	6	VXI_A3
7	GND	8	VXI_A4
9	GND	10	VXI_A5
11	GND	12	VXI_A6
13	GND	14	VXI_A7
15	GND	16	VXI_A8
17	NO PIN	18	NO PIN
19	GND	20	VXI_A9
21	GND	22	VXI_A10
23	GND	24	VXI_A11
25	GND	26	VXI_A12
27	GND	28	VXI_A13
29	GND	30	VXI_A14
31	GND	32	VXI_A15
33	GND	34	VXI_A16
35	NO PIN	36	NO PIN
37	GND	38	VXI_A17
39	GND	40	VXI_A18
41	GND	42	VXI_A19
43	GND	44	VXI_A20
45	GND	46	WR*
47	GND	48	CLK_IN
49	GND	50	WGATE*
51	GND	52	WRSTR
53	NO PIN	54	NO PIN
55	GND	56	+5V_A_OK
57	GND	58	-5V_A_OK
59	GND	60	+12V_OK
61	GND	62	-12V_OK
63	GND	64	+5V_OK
65	GND	66	+2.5V_D_OK
67	GND	68	+3.3V_D_OK
69	GND	70	-2VD_OK

VXI Data and TTLTRG Bus—J3			
SAMTEC P/N ASP-32646-01			
Pin	Name	Pin	Name
1	GND	2	VXI_D0
3	GND	4	VXI_D1
5	GND	6	VXI_D2
7	GND	8	VXI_D3
9	GND	10	VXI_D4
11	GND	12	VXI_D5
13	GND	14	VXI_D6
15	GND	16	VXI_D7
17	NO PIN	18	NO PIN
19	GND	20	VXI_D8
21	GND	22	VXI_D9
23	GND	24	VXI_D10
25	GND	26	VXI_D11
27	GND	28	VXI_D12
29	GND	30	VXI_D13
31	GND	32	VXI_D14
33	GND	34	VXI_D15
35	NO PIN	36	NO PIN
37	GND	38	TTLTRG0
39	GND	40	TTLTRG1
41	GND	42	TTLTRG2
43	GND	44	TTLTRG3
45	GND	46	TTLTRG4
47	GND	48	TTLTRG5
49	GND	50	TTLTRG6
51	GND	52	TTLTRG7
53	NO PIN	54	NO PIN
55	GND	56	TTLTRG_OUT0
57	GND	58	TTLTRG_OUT1
59	GND	60	TTLTRG_OUT2
61	GND	62	TTLTRG_OUT3
63	GND	64	TTLTRG_OUT4
65	GND	66	TTLTRG_OUT5
67	GND	68	TTLTRG_OUT6
69	GND	70	TTLTRG_OUT7



FOARC and Diagnostic—J7			
SAMTEC P/N ASP-32646-01			
Pin	Name	Pin	Name
1	GND	2	FOARC00
3	GND	4	FOARC01
5	GND	6	FOARC02
7	GND	8	FOARC03
9	GND	10	FOARC04
11	GND	12	FOARC05
13	GND	14	FOARC06
15	GND	16	FOARC07
17	NO PIN	18	NO PIN
19	GND	20	FOARC08
21	GND	22	FOARC09
23	GND	24	FOARC10
25	GND	26	FOARC11
27	GND	28	FOARC12
29	GND	30	FOARC13
31	GND	32	RST_OUT
33	GND	34	TST_OUT
35	NO PIN	36	NO PIN
37	GND	38	TEST_DATA00
39	GND	40	TEST_DATA01
41	GND	42	TEST_DATA02
43	GND	44	TEST_DATA03
45	GND	46	TEST_DATA04
47	GND	48	TEST_DATA05
49	GND	50	TEST_DATA06
51	GND	52	TEST_DATA07
53	NO PIN	54	NO PIN
55	GND	56	TEST_DATA08
57	GND	58	TEST_DATA09
59	GND	60	TEST_DATA10
61	GND	62	TEST_DATA11
63	GND	64	TEST_DATA12
65	GND	66	TEST_DATA13
67	GND	68	TEST_DATA14
69	GND	70	TEST_DATA15

FLASH and History Buffer Controls—J8			
SAMTEC P/N ASP-32646-01			
Pin	Name	Pin	Name
1	GND	2	FL_DCLK
3	GND	4	FL_OE
5	GND	6	FL_WE#
7	GND	8	FL_PGM0
9	GND	10	FL_TCK
11	GND	12	FL_RY/BY#
13	GND	14	FL_INIT_CONF
15	GND	16	FL_PGM1
17	NO PIN	18	NO PIN
19	GND	20	FL_TDI
21	GND	22	FL_RP#
23	GND	24	FL_TMS
25	GND	26	FL_PGM2
27	GND	28	FL_DATA0
29	GND	30	FL_nCS
31	GND	32	FL_CE#
33	GND	34	FL_OE#
35	NO PIN	36	NO PIN
37	GND	38	HB_OER
39	GND	40	HB_RWR
41	GND	42	HB_CSR
43	GND	44	HB_BSY_R
45	GND	46	HB_BSY_L
47	GND	48	HB_CSL
49	GND	50	HB_RWL
51	GND	52	HB_OEL
53	NO PIN	54	NO PIN
55	GND	56	PLD_TDO
57	GND	58	RF_FLT
59	GND	60	RF_PERMIT
61	GND	62	WDOG
63	GND	64	MUX_1
65	GND	66	MUX_2
67	GND	68	SRST*
69	GND	70	SPARE



ADC Control—J13			
SAMTEC P/N ASP-32646-01			
Pin	Name	Pin	Name
1	GND	2	DB_0
3	GND	4	DB_1
5	GND	6	DB_2
7	GND	8	DB_3
9	GND	10	DB_4
11	GND	12	DB_5
13	GND	14	DB_6
15	GND	16	DB_7
17	NO PIN	18	NO PIN
19	GND	20	DB_8
21	GND	22	DB_9
23	GND	24	DISP_LD
25	GND	26	CLK_20MHZ
27	GND	28	CONVST*
29	GND	30	RF_PERMIT_LR_SW
31	GND	32	CLK_40_SEL
33	GND	34	CLK_40_INT
35	NO PIN	36	NO PIN
37	GND	38	BUSY0
39	GND	40	BUSY1
41	GND	42	BUSY2
43	GND	44	BUSY3
45	GND	46	BUSY4
47	GND	48	BUSY5
49	GND	50	BUSY6
51	GND	52	BUSY7
53	NO PIN	54	NO PIN
55	GND	56	CS0
57	GND	58	CS1
59	GND	60	CS2
61	GND	62	CS3
63	GND	64	CS4
65	GND	66	CS5
67	GND	68	CS6
69	GND	70	CS7

5.10.7 On-Board Calibration Display

There is a three-position, seven-segment display on the HPM board that assists in calibration of the HPM. In addition, there are individual LEDs that indicate which channel is being



calibrated. Individual channel selection is via a push-button switch processed by the Altera PLD. The calibration mode is selected via a jumper on the board.

5.11 HPM EPICS Parameters

All features and functions of the HPM (except those specifically excluded) are accessible through the VXIbus interface, accessed via EPICS.

Switches are provided on the HPM to assert the TTLTRG5* (RF_PERMIT_L), TTLTRG2* (RF_PERMIT_C), or the TTLTRG7* (RF_PERMIT_R) line, but not all simultaneously. The positions of the switches are readable via EPICS.

The HPM implements a read-after-write and read-on-demand function for the EPICS interface for all settable parameters. Parameters are volatile (lost on power-down). If power is cycled on the HPM, it will signal to EPICS that the parameter files need to be reloaded.

Tables 5-8, 5-9, and 5-10 map the registers used to communicate between the HPM and EPICS.

Table 5-8. HPM Data Register Descriptions

VXI Address = 0xF00 80000 + Byte Offset from the table below.

- *The 0xF00 is set by VXWorks on boot-up and depends on the system configuration.*
- *The 80000 is set by the A24 base address = A16 offset (see Table 5-10), shifted left by 16 bits.*

Byte Offset (Hex)	Word Offset (Decimal)	EPICS Variable Name	HPM Data Register Description
0x00	0	ADC_ERR	Error word (one bit per channel) indicating an ADC error. Bits 00 --> 07: ADC Channel 0 --> 7, which overflowed (reached 3FF _h). Bits 08 --> 15: ADC Channel 0 --> 7, which failed ADC_SLF_TST. EPICS read/clear
0x02-10	2-8	ADC_BASELINE_[0..7]	Zero value of ADC channels sampled ADC_BASELINE_DLY μ s after PREPULSE (while RF is off). Bits 00 --> 09: ADC Data (10 bits) Bits 10 --> 15: Not used EPICS read only
0x12	9	ADC_BASELINE_DLY	Time delay in μ s from falling edge of PREPULSE to latch all ADC_BASELINE_XX values while RF_GATE is off. Used to measure zero offset of each RF channel. Same delay for all channels. EPICS write/read



Byte Offset (Hex)	Word Offset (Decimal)	EPICS Variable Name	HPM Data Register Description
0x14-22	10-17	ADC_DATA_[0..7]	Time-synchronized data from ADC with ADC_BASELINE_XX subtracted from it. This is the corrected data used for all HPM decisions; it is what is reported to EPICS. Bits 00 --> 09: ADC Data (10 bits) Bits 10 --> 15: Not used EPICS read only
0x24-32	18-25	ADC_SAMPLE_[0..7]	Corrected ADC_DATA latched on the falling edge of SAMPLE*. Read by EPICS, overwritten by next SAMPLE* command. Bits 00 --> 09: ADC Data (10 bits) Bits 10 --> 15: Not used EPICS read only.
0x34	26	ADC_SLF_TST_DLY	Time in μ s from falling edge of RF_GATE* to latch data for self-test (same for all channels). Should be less than FILL_TIME (1 --> 511 μ s). Used to detect broken cable and/or stuck-at-zero faults on ADC. EPICS write/read
0x36-44	27-34	ADC_SLF_TST_VAL_[0..7]	Threshold that the ADC data must exceed at ADC_SLF_TST_DLY to be OK (may be different for each channel). Bits 00 --> 09: ADC_SLF_TST_VAL (10 bits) Bits 10 --> 15: Not used EPICS write/read
0x46	35	BACKPLANE	Two-byte flag indicating status of TTLTRG* bus and miscellaneous data (1 = OK; 0 = FLT). Bit 00: TTLTRG0* (SAMPLE*) Bit 01: TTLTRG1* (SRF_TUNE*) Bit 02: TTLTRG2* (RF_PERMIT_C) Bit 03: TTLTRG3* (RF_GATE*) Bit 04: TTLTRG4* (PREPULSE) Bit 05: TTLTRG5* (RF_PERMIT_L) Bit 06: TTLTRG6* (MPS_PERMIT) Bit 07: TTLTRG7* (RF_PERMIT_R) Bit 08: RF_PERMIT_HARD (Optoisolated hardware input readout) Bit 09: CAV_OK (Cavity Power OK after FILL_TIME) Bit 10: FOARC_FLT Bit 11: Not used Bit 12: Not used Bit 13: Not used Bit 14: Not used Bit 15: DATA_REG_LOST*. Need to reload EPICS parameters. Cleared on power-up, set by EPICS after registers are reloaded. EPICS write bit 15 only/read all
0x48	36	BOARD_REV	Two bytes used to define board hardware version and serial number. Different from firmware version encoded in PLD_REV. Bits 00--> 04: Board hardware revision level (01 --> 32). Bits 05--> 14: Board serial number, starts at 00 with each new hardware revision. Bit 15: Zero always.



Byte Offset (Hex)	Word Offset (Decimal)	EPICS Variable Name	HPM Data Register Description
0x4A	37	DIAGMUX_CNTL	<p>Two-byte word to control the diagnostic multiplexers. See Table 5-5 for channel assignments.</p> <p>Bit 00: DIAGMUXA_A0 Bit 01: DIAGMUXA_A1 Bit 02: DIAGMUXA_A2 Bit 03: DIAGMUXA_A3 Bit 04: DIAGMUXB_A0 Bit 05: DIAGMUXB_A1 Bit 06: DIAGMUXB_A2 Bit 07: DIAGMUXB_A3 Bit 08: Not used Bit 09: Not used Bit 10: LBUS_S0 (Controls LBUS exchange switch) Bit 11: LBUS_S1 Bit 12: LBUS_S2 Bit 13: 1 = Disable baseline subtract of ADC values (ADC_BASELINE_0..7). Bit 14: 1 = Freeze history buffer at the end of the next macropulse. Bit 15: 1 = Freeze history buffer at the end of the next macropulse that has a SAMPLE* event.</p> <p>EPICS write/read</p>
0x4C	38	FAULT	<p>RF Fault word to EPICS: 1 = OK; 0 = FLT on each bit. On any HPM-generated fault, the IOC reads this register to determine the type of fault. This is a pointer to the more-detailed fault-status registers.</p> <p>Bit 00 --> 07: Channel number of RF fault Bit 08: FOARC Fault Bit 09: RF_PERMIT_L (TTLTRG5*) Bit 10: MPS_PERMIT (TTLTRG6*) Bit 11: RF_PERMIT_R (TTLTRG7*) Bit 12: RF_PERMIT_C (TTLTRG2*) Bit 13: RF_PERMIT_HARD = 0 Bit 14: ADC_ERR set Bit 15: HDWR_STATUS error (power supplies or external 40-MHz clock)</p> <p>EPICS read only</p>
0x4E	39	FILL_TIME	<p>Duration from RF_GATE* on (in μs) to ignore all RF FAULTS (but not FOARC faults). Same value for all RF channels. 1 < Value < 511 μs. Typical for NC: 10 μs; typical for SRF: 250 μs</p> <p>NORM: EPICS write/read</p>
0x50	40	FOARC_FLT	<p>Two-byte register to show which FOARC channel faulted. Set on PREPULSE*.</p> <p>Bits 00 --> 13: FOARC Channel 13 --> 00 faulted (low = Fault) Bit 14: Not used Bit 15: 1 = OK; 0 = Bit 15 of one of the FOARC_HIST counters has been set and is about to overflow (come read me).</p> <p>EPICS read only</p>
0x52-6C	41-54	FOARC_HIST_[0..13]	<p>Sixteen-bit counter for each FOARC channel. Lost on power-down.</p> <p>EPICS read/clear</p>
0x6E	55	FOARC_MASK	<p>Two-byte mask for FOARC channels: 1 = Enable channel; 0 = Ignore.</p> <p>Bit 00 --> 13: Mask to ignore FOARC Channels 00 --> 13 Bit 14: 1 = Set FOARC chassis reset; 0 = Clear (FOARC_RST) Bit 15: 1 = Set FOARC lamp test; 0 = Clear (FOARC_TST)</p> <p>EPICS write/read</p>



Byte Offset (Hex)	Word Offset (Decimal)	EPICS Variable Name	HPM Data Register Description
0x70	56	HDWR_STATUS	<p>Two-byte flag for HPM hardware status: 1 = OK; 0 = Fault.</p> <p>Bit 00: Not used Bit 01: Not used Bit 02: Not used Bit 03: LCR Bit 0: 00 = Right, 10 = Center, 01 = Left, 11 = Not Allowed Bit 04: LCR Bit 1: 00 = Right, 10 = Center, 01 = Left, 11 = Not Allowed Bit 05: +2.5VREF_OK Bit 06: -12VA_OK Bit 07: -5.VA_OK Bit 08: -2VD_OK Bit 09: +2.5VD_OK Bit 10: +3.3VD_OK Bit 11: +5VD_OK Bit 12: +5VA_OK Bit 13: +12VA_OK Bit 14: 40-MHz Clock status (RO): 0 = External; 1 = Internal clock used Bit 15: Not used (always 1)</p> <p>EPICS read only</p>
0x72	57	HISTBUFF_SRC	<p>Two-byte source-channel-select for history buffer source data. See Section 5.7.</p> <p>Table 5-9 shows the signal source for buffers A and B.</p> <p>EPICS write/read</p>
0x74	58	PLD_REV	Revision level for PLD firmware.
0x76	59	PROM_ADDR	<p>Address to 64-K page in Altera reprogramming PROM to allow reprogramming via EPICS.</p> <p>Bits 00 --> 04: PROM Address Lines A17 --> A21 Bits 05 --> 07: PROM PGM_A[0..2] (Selects the page in PROM from which to program the PLD.) PGM_A0 = Bit 05) Bits 08 --> 15: Not used</p>
0x78-86	60-67	RF_DLY_HI[0..7]	<p>Persistence (in μs) for which a high-power fault must exist (after FILL_TIME) prior to declaring a fault. Individually set for each channel.</p> <p>EPICS write/read</p>
0x88	68	RF_MASK	<p>Two-byte mask for RF channel enable: 1 = Enable; 0 = Ignore channel.</p> <p>Bits 00 --> 07: Mask off RF channels 00 --> 07 Bits 08 --> 14: Not used Bit 15: RF_PERMIT_SOFT. Provides RF_PERMIT input for EPICS. Both RF_PERMIT_HARD (front panel hardware input) and RF_PERMIT_SOFT must be set to permit RF operations. The system may be tested by clearing RF_PERMIT_SOFT and seeing that the proper fault is asserted.</p> <p>EPICS write/read</p>
0x8A-98	69-76	RF_SET_HI[0..7]	<p>High setpoint for setting an RF fault, which persists for RF_DLY_HI μs. Individually set for each channel.</p> <p>EPICS write/read</p>
0x9A	77	SRF_TUNE_DLY	<p>Time in μs in which to ignore all RF faults (but not FOARC faults) on falling edge of TTLTRG1* (SRF_TUNE*). Used during SRF tuning only. 1 < Value < 512 μs.</p> <p>EPICS write/read</p>
0x9C	78	FOARC_RST	Resets all FOARC counters
0x9E	79	LIRQ_CLR	Clears all local interrupt requests (LIRQs).
0xA0-A2	80-81	BOARD_ID	Reads "HPM" on EPICS screen.



Table 5-9. Source Signals for Buffers A and B

Low Byte – Signal Source for Buffer A				High Byte – Signal Source for Buffer B			
Value	Signal	Value	Signal	Value	Signal	Value	Signal
00	TTLTRG0*	10	FOARC_00	00	TTLTRG0*	10	FOARC_00
01	TTLTRG1*	11	FOARC_01	01	TTLTRG1*	11	FOARC_01
02	TTLTRG2*	12	FOARC_02	02	TTLTRG2*	12	FOARC_02
03	TTLTRG3*	13	FOARC_03	03	TTLTRG3*	13	FOARC_03
04	TTLTRG4*	14	FOARC_04	04	TTLTRG4*	14	FOARC_04
05	TTLTRG5*	15	FOARC_05	05	TTLTRG5*	15	FOARC_05
06	TTLTRG6*	16	FOARC_06	06	TTLTRG6*	16	FOARC_06
07	TTLTRG7*	17	FOARC_07	07	TTLTRG7*	17	FOARC_07
08	ADC_IN0	18	FOARC_08	08	ADC_IN0	18	FOARC_08
09	ADC_IN1	19	FOARC_09	09	ADC_IN1	19	FOARC_09
0A	ADC_IN2	1A	FOARC_10	0A	ADC_IN2	1A	FOARC_10
0B	ADC_IN3	1B	FOARC_11	0B	ADC_IN3	1B	FOARC_11
0C	ADC_IN4	1C	FOARC_12	0C	ADC_IN4	1C	FOARC_12
0D	ADC_IN5	1D	FOARC_13	0D	ADC_IN5	1D	FOARC_13
0E	ADC_IN6	1E	RF_PERMIT_HARD	0E	ADC_IN6	1E	RF_PERMIT_HARD
0F	ADC_IN7	1F	MPS_PERMIT	0F	ADC_IN7	1F	MPS_PERMIT



Table 5-10. HPM A16 Address Space

Base Address = 0xC000 + Logical Address shifted 6 bits left.

Logical address is set by rotary Dual-Inline-Package (DIP) switches on VXIbus-interface circuit. See also Table 5-8.

Data courtesy of Kay-Uwe Kasemir 09/13/01

Byte offset from A16 base, Read/Write	A16 ADDRESS [HPM Default]
0, R	MANUFACTURER ID [4FA0 _h] Bits 00 --> 11: Manufacturer ID [FA0 _h] (LANL) Bits 12 --> 13: Address Space [00 ₂] (have A16 and A24) Bits 14 --> 15: Device Class [01 ₂] (Extended Register Based)
0, W	LOGICAL ADDRESS Bits 00 --> 07: Logical Address selected via rotary switches.
2, R	DEVICE TYPE: [FF4C] Bits 00 --> 11: Model code [F4C] (3916 _d) Bits 12 --> 15: Required Memory, encoded in an unusual way: 2 ^{^(23-memory)} . 1111 = 256 bytes 0000 = 8388608 bytes
4, R	STATUS Bit 00: 0 = 402.5 MHz build; 1 = 805 MHz build Bit 01: Not used Bit 02: 1 = Passed self-test; 0 = Failed/busy Bit 03: 1 = Ready; 0 = Register-initialization failed. Bits 04 --> 13: Device-dependent Bit 14: MODID*: 1 = Device not selected; 0 = Device selected Bit 15: A24/A35 Active. Cleared on SYSRESET*, set by A24/A32 Enable bit in Control Register.
4, W	CONTROL Bit 00: Reset: 1 = Reset; 0 = Normal Bit 01: SYSFAIL Inhibit: 1 = Do not assert SYSFAIL*; 0 = SYSFAIL* permitted. Bits 02 --> 12: Device-dependent (Not used) Bit 13: SINT. One -zero transition generates an interrupt for testing. Bit 14: Not used Bit 15: A24/A32 Enable: 1 = Permit; 0 = Deny
6, RW	OFFSET (RD/WR) Bits 00 --> 15: A24 Memory offset address bits 23 --> 8. Allows locating the A24 base address of this board in increments of 0 x FF.



Byte offset from A16 base, Read/Write	A16 ADDRESS [HPM Default]
8, R	ATTRIBUTE Bit 0=0: Device implements the interrupt-control registers (see 0x1C,RW). Bit 1=1: This device is not an interrupt handler. Bit 3=0: This device has interrupt-status reporting capability (see 0x1A,R). Rest: Reserved
0x0A, 0x0C, R	SERIAL HIGH, LOW
0x1A, R	INTERRUPT STATUS Bits 8-15: One bit for each local interrupt-request line. This byte is the high byte of the VXIbus 16-bit interrupt vector. Reading this byte will <i>not</i> clear the interrupt; some other register in the board has to be read to clear the interrupt request (i.e., drop the local interrupt-request line). Rest: Reserved
0x1C, RW	INTERRUPT CONTROL Bits 00 --> 02: Interrupt-Handler Level* 111. Bits 03 --> 05: Interrupt-Request (IRQ) Level*: 000=Use level 7; 001=Use level 6. Bit 06: Interrupt-Handler Enable* (= 1 always because this board does not handle interrupts) Bit 07: Interrupt-Request Enable* (0 = Enable IRQ): CPU sets this when it's ready to receive interrupts from this board. Bit 08: IRQ0* (0 = IRQ) Bit 09: IRQ1* Bit 10: IRQ2* Bit 11: IRQ3* Bit 12: IRQ4* Bit 13: IRQ5* Bit 14: IRQ6* Bit 15: IRQ7*: 1 = Disable local interrupt line 7; 0 = Enable local interrupt line 7.



5.12 HPM Power Requirements **TBD**

+24 VDC

+5 VDC

+12 VDC

-2 VDC

-5.2 VDC

-12 VDC

-24 VDC