

Date: Wed, 24 May 2000 16:36:53 -0600
From: ron@lanl.gov (Ron Nelson)
Subject: Re: T0 generation, revised
To: Larry Doolittle <lloodlitt@recycle.lbl.gov>, Tom Shea <shea@ornl.gov>, Brian Oerter <oerter@bnl.gov>
Cc: Bill DeVan <devanwr@ornl.gov>, Dave Gurd <gurd@lanl.gov>, dabernathy@anl.gov (Doug Abernathy)

The Cerro Grande wildfire delayed my response to Larry's email, which was triggered by last month's timing review in Oak Ridge.

Larry's idea of generating the ring rf with the reference timing box is really interesting. And if you extend it a little you can get what could be an interesting "trigger" mode of operation for the accelerator and the neutron choppers. I thought I'd try this notion out on you folks and see what possible technical and political problems you expect might arise. Here goes.

I think it would be interesting to consider a mode where the chopper system triggers the accelerator, and thereafter the accelerator looks like a delay line to the chopper, target, and spectrometer systems. Suppose it is possible for the choppers to generate two timing pulses in advance of beam on target. For example, the first "pre-trigger" might come 3333.3 ± 0.2 us before beam is delivered to the target. This time is arbitrary but the error must be fairly small. The second "trigger" pulse might come 1666.7 ± 0.1 us before beam on target. Conceptually these two timing pulses are very like pulses in the current scheme except the choppers are providing these two very significant timing markers, not the grid via the filtered 600 Hz. Note that these are fixed absolute delays--no "breathing" here. (The choppers are following the filtered 60 Hz timing reference derived from the grid exactly as discussed last month.)

The pre-trigger pulse signals the reference timing generator to make any phase shifts that might be required to get the ring rf matched to the expected chopper trigger pulse. We can use Larry's algorithm to adjust the phase of the ring rf. The proposed scenario nominally has 1587 1.05-MHz cycles for any required phase change, which is obviously limited to half a cycle. Later if the trigger pulse is not precisely in phase with the ring rf signal, then the reference timing controller has one last chance to further shift the phase of the ring rf during the next 500 us. This shift should be small thanks to the pre-trigger event. Upon receipt of the trigger event, we know by design the number of ring rf cycles before the beam is on target. The number of cycles need not be an integer. During the 1100-1200 us prior to beam on target the phase of the ring rf is not shifting so the period is fixed as required for ring operation with beam.

Using the timing system protocols that measure course time in ring rf cycles, the accelerator starts its master timer sequence with the goal of having beam on target 1666.7 us later. It gets the RF cavities ready for beam, loads the ring, and extracts the pulse in an optimum sequence with the only constraint that beam arrives on target 1666.7 us after the trigger. With this protocol the ring loading can be initiated such that the number of orbits after loading is completed can be minimized. This eliminates YY's concern. Furthermore this eliminates the ± 0.5 us jitter for extracting beam since extraction is planned before the ring is loaded.

We have looked at some simulations and see what problems arise when we try to forecast chopper top-dead-center 3 ms in advance. It looks be dead easy. The interval between a 3.3 ms pre-trigger and the actual chopper top-dead-center arrival time exhibits only a 25 ns jitter for a "worst

case" chopper operating at 20 Hz. Here the simulation includes a chopper with controller following our measured power grid with real fluctuations. The more significant problem will be the multiple chopper issue, I suspect.

This trigger mode of operation is applicable only when the frequency content of the power grid has been low-pass filtered such that the choppers are doing only a "fair" job of tracking grid changes, and some high frequency jumps in the power grid demand additional high-frequency compensation. Ultimately a lower frequency cutoff offers an alternate mode where both the accelerator and choppers can follow the timing reference signals without feedback from the choppers to the accelerator. While this mode might be desirable due to its simplicity, the phase of the filtered 60 Hz deviates more from the actual phase of the power grid. The trigger mode reduces this difference and thus may be of interest.

Clearly this notion of accelerator triggering is out of scope but it's fun to explore the feasibility.

Later.
Ron.

PS--LANSCE survived the fire without damage.

At 11:00 AM 4/20/00 -0700, Larry Doolittle wrote:

>Guys -

>

>This description is slightly cleaned up and expanded from the
>version I rushed out yesterday. The concept is exactly the same.

>

>You can build a perfect generator of T0, Text, and Ring RF in a
>small FPGA (with a supporting DAC and filter). Here's how, using
>a slightly tweaked DDS architecture. The Ring RF can optionally
>be phase locked to the Text output.

>

>n = number of reference clock cycles in the next "60 Hz" period
> typical at 80 MHz, 1333333

>

>m = number of 1.05 MHz (nominal) clock cycles in next "60 Hz" period
> typical 17637

>

>p = number of bits in phase accumulator
> typical 24

>

>s = 1.05 MHz phase advance desired in next "60 Hz" period,
> units of phase accumulator bits
> typical 0

>

>k = coarse 1.05 MHz phase advance per clock cycle,
> units of phase accumulator bits
> $(m \cdot (2^p) + s) / n$
> typical 221924

>

>l = number of extra lsb units (carry in) to complete phase advance
> $(m \cdot (2^p) + s) \% n$
> $m \cdot (2^p) + s - n \cdot k$
> typical 1165900

>

>q = number of 1.05 MHz RF cycles T0 leads Text

> typical 1600
>
>Need a 22 bit (typical, guaranteed greater than $1+\ln 2(n)$) adder
>that implements the standard graphics line-drawing algorithm:
> $t = t + (t > 0) ? (l - n) : l$. The carry in to p-bit phase accumulator
>is $(t > 0)$. I use that expression instead of the more conventional
> $t = t + l - (t > n) ? n : 0$ to keep the number of 80 MHz adders to a
>minimum.
>
>In concept, every new "60 Hz" period could latch in new values
>for n, k, l, and l-n. n is the appropriately filtered output
>of the line monitor. If you wanted to hit a given RF phase at
>the time of the next rollover, set s to (target-current). If
>you don't want to run phase locked like that, a constant value
>of s is effectively a fine frequency control.
>
>All of that exotic 40-bit integer arithmetic above (including
>division) only needs to be done at 60 Hz. I would assume that
>would be done in the same micro/DSP that handles the line voltage
>acquisition, filtering, and zero crossing finder.
>
>This implementation gives you everything you need to put out
>a trigger pulse T0 which is q (typically about 1600) cycles
>of 1.05 MHz RF before the next Text, with a jitter of 12 ns.
>Once the phase delay of the DDS cosine, DAC, and analog
>filter is characterized, and the output is synched with the
>16X clock, jitter turns effectively to zero. Given one
>counter that rolls over at n, you need to compare that value
>against $n - q * n / m$ to generate T0.
>
>I chose 80 MHz, the synchronous logic clock rate, almost at
>random. It should be a multiple of 10 MHz, to allow easy
>generation from a 10 MHz frequency standard. It needs to be
>somewhat larger than $32 * 1.05$ MHz, so the trigger synchronizer
>can work without adding jitter (once the system is tuned,
>and the RF is running phase locked). Finally, the FPGA has
>to be able to do 24-ish bit arithmetic at that rate. I know
>the Xilinx Virtex has no problem doing that at 80 MHz, but if
>I were to prototype this on the Spartan-1 gear I have on hand,
>I would have to slow it down some.
>
>I realize this description leaves plenty of details to your
>imagination. I wanted to point out that perfect timing is not
>only theoretically possible, but can be implemented cleanly.
>
> - Larry

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